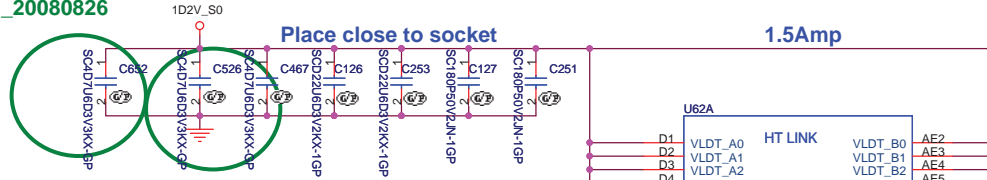
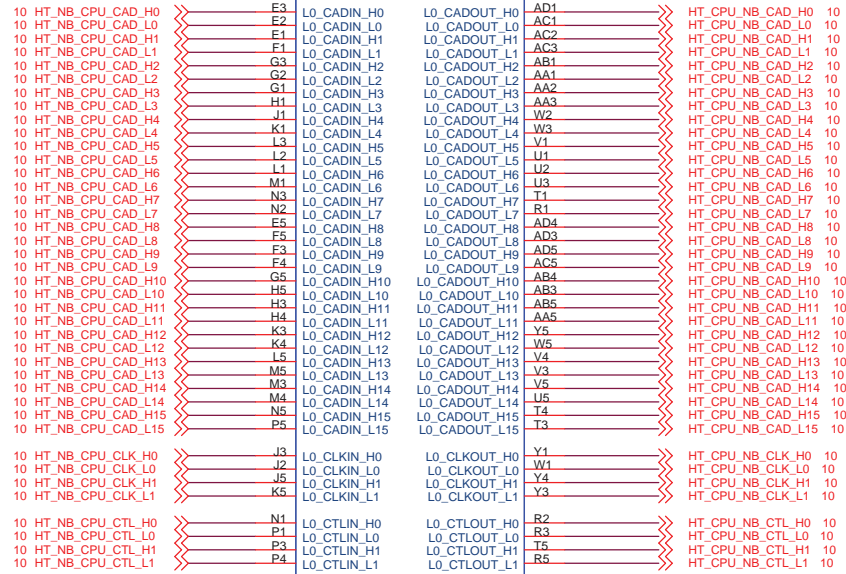


SB_20080826



SA_20080723

State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

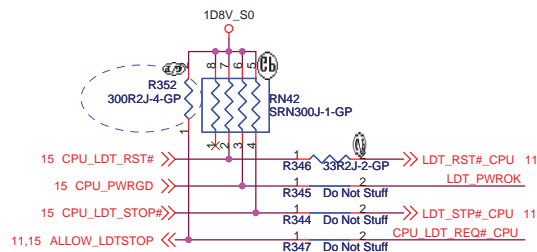
SKT-CPU638P-GP-U2
62.10055.111 2ND = 62.10055.251

SKT-BGA638H176

MP

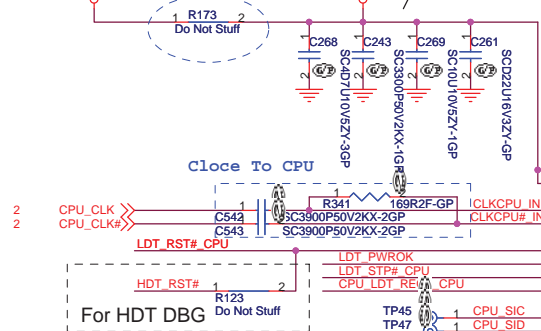
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title				
CPU_HT_LINK I/F_(1/4)				
Size	Document Number			Rev
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Date: Thursday, October 09, 2008		Sheet	3	of 47

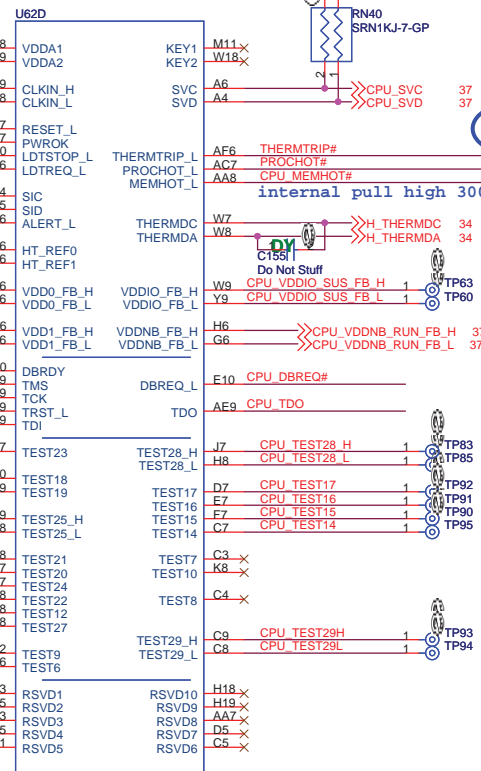
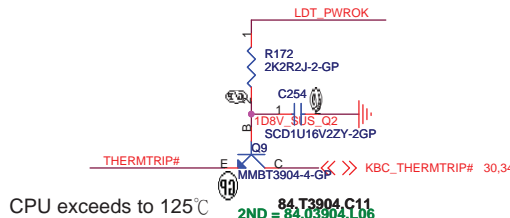
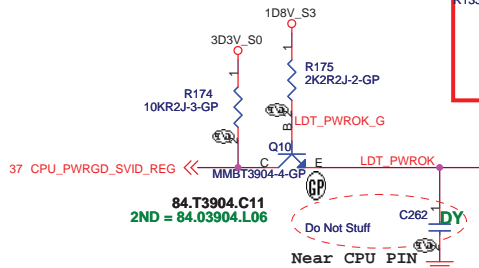
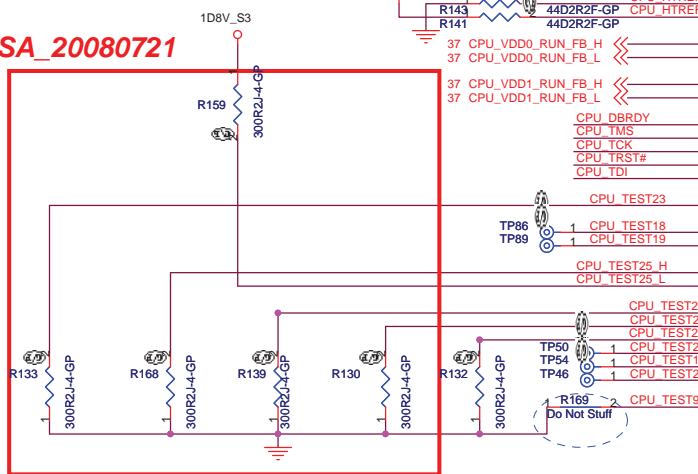


IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

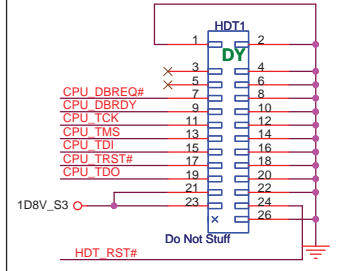


SA_20080721

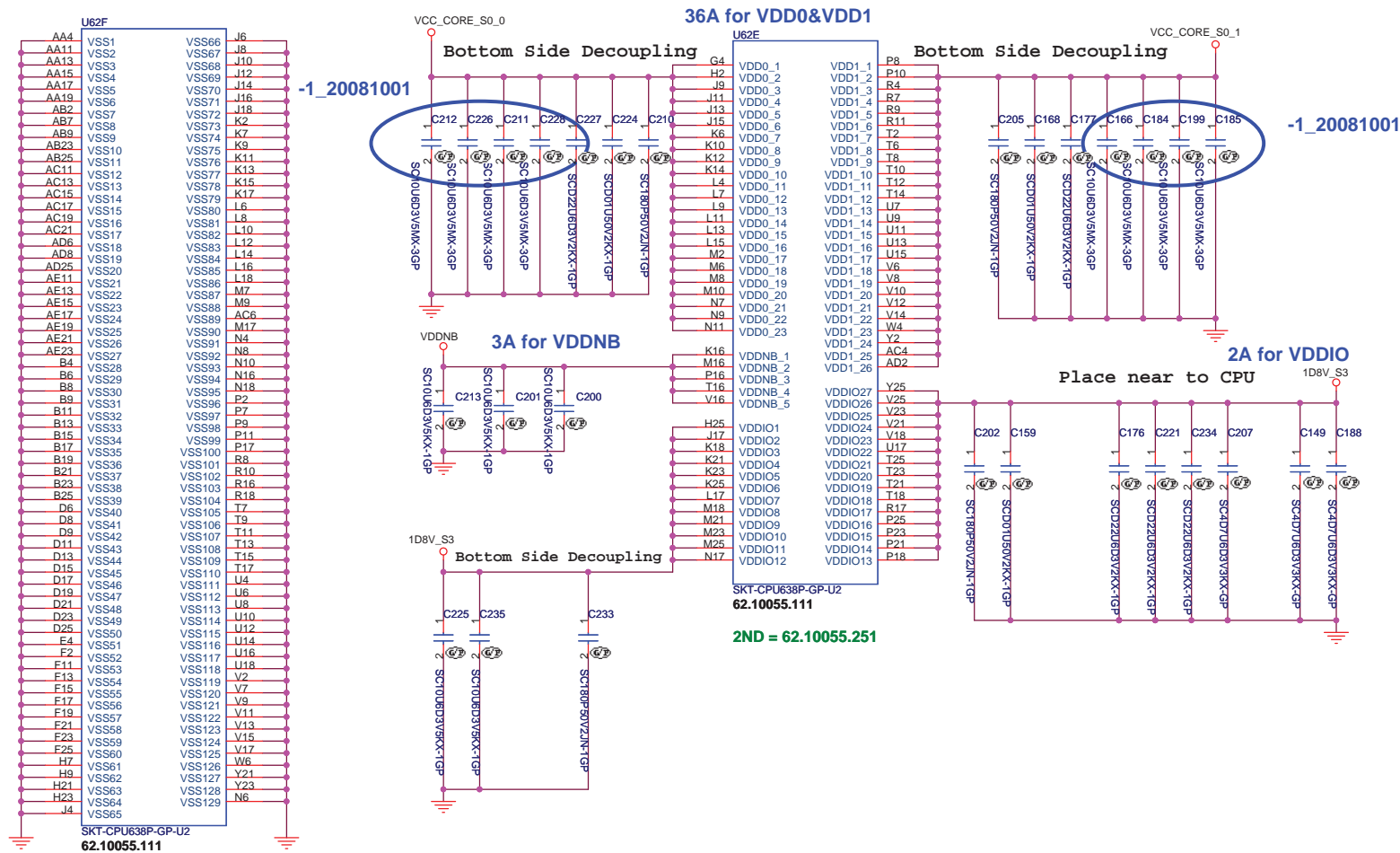


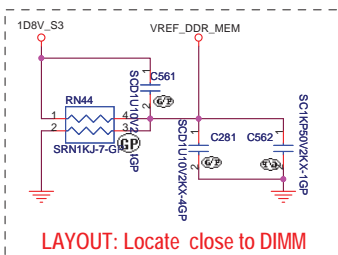
LAYOUT: Route FBCLKOUT_H/L
differentially impedance 80

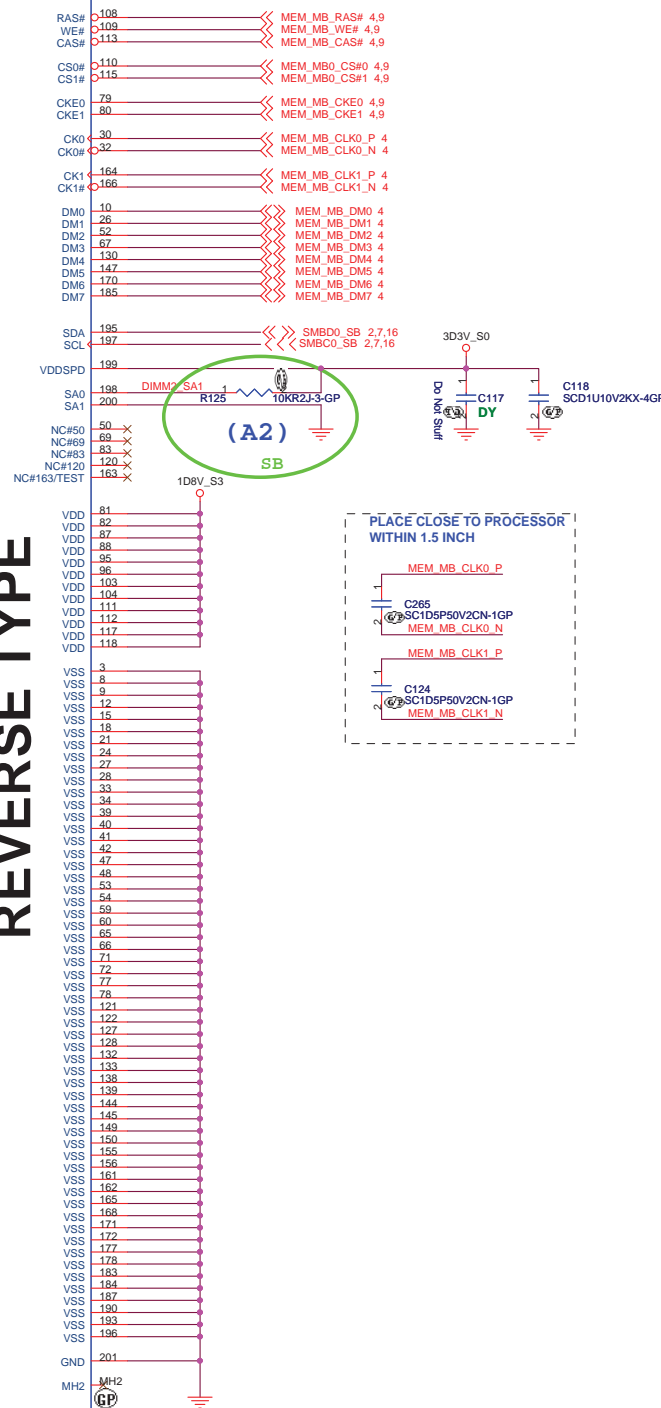
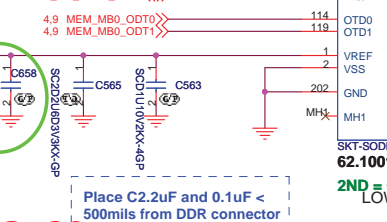
HDT Connectors



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PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH

MEM MB CLK0_P

C265
SC1D5P50V2CN-1GP

MEM MB CLK0_N

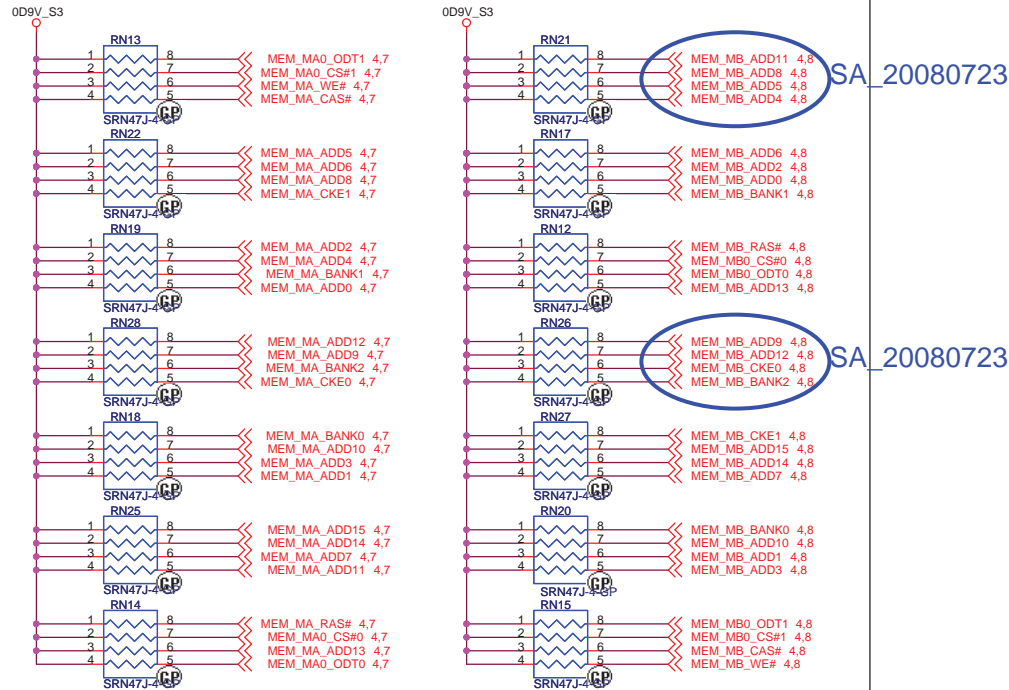
MEM MB CLK1_P

C124
SC1D5P50V2CN-1GP

MEM MB CLK1_N

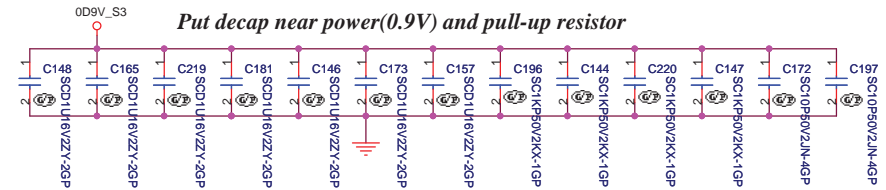
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

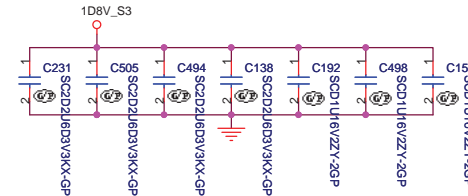


Do not share the Term resistor between the DDR address and Control Signals.

Decoupling Capacitor

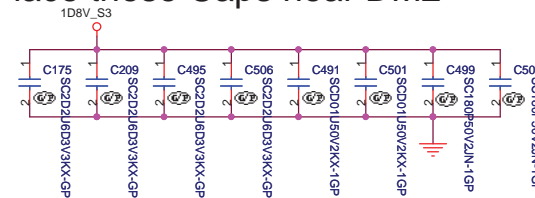


Place these Caps near DM1

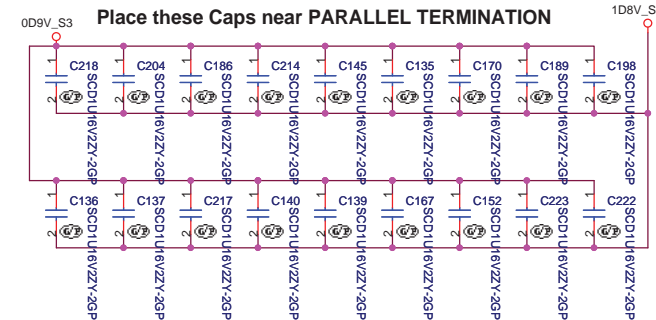


Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0.9V_S3

Place these Caps near DM2



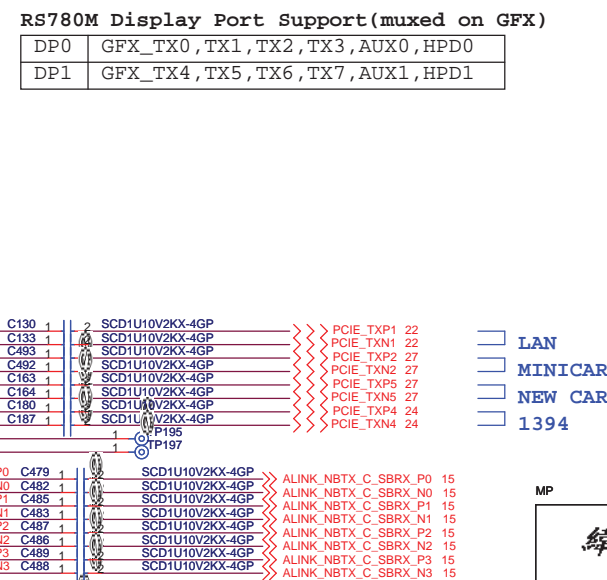
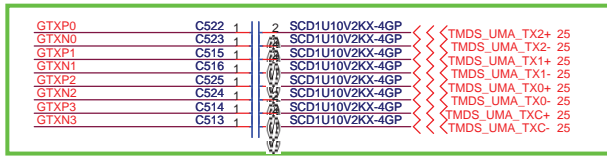
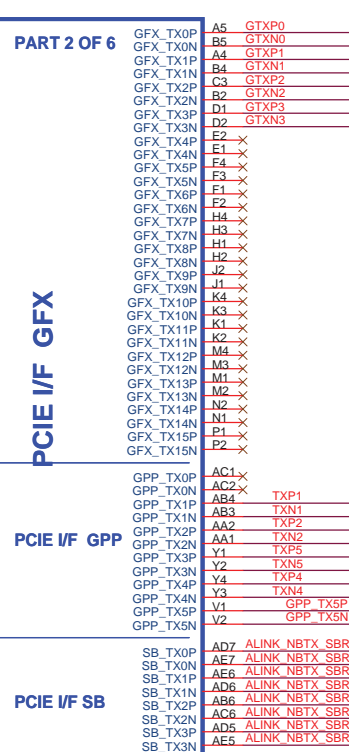
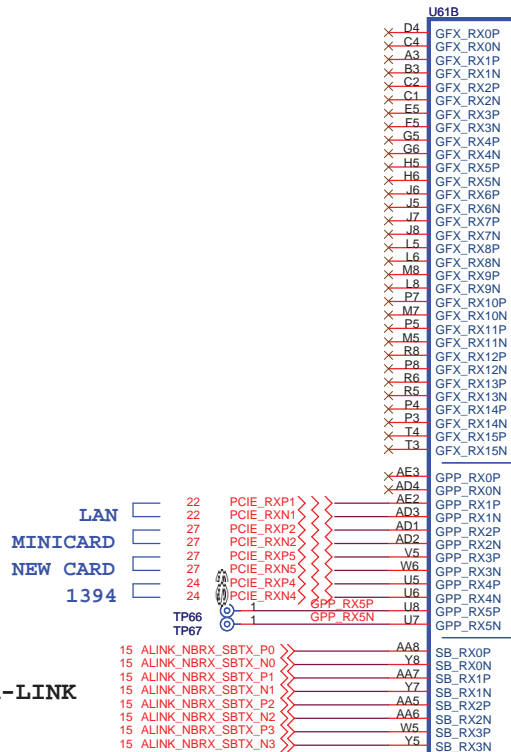
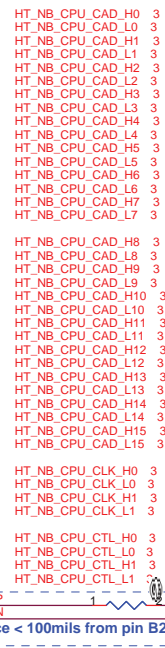
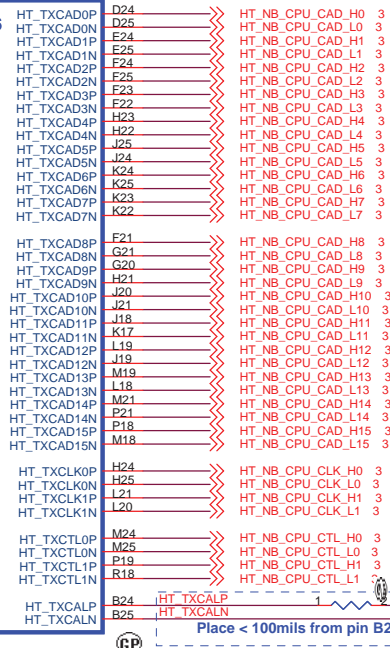
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0.9V_S3



MP

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Title		
DDR DAMPING & TERMINATION		
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F7-GT		
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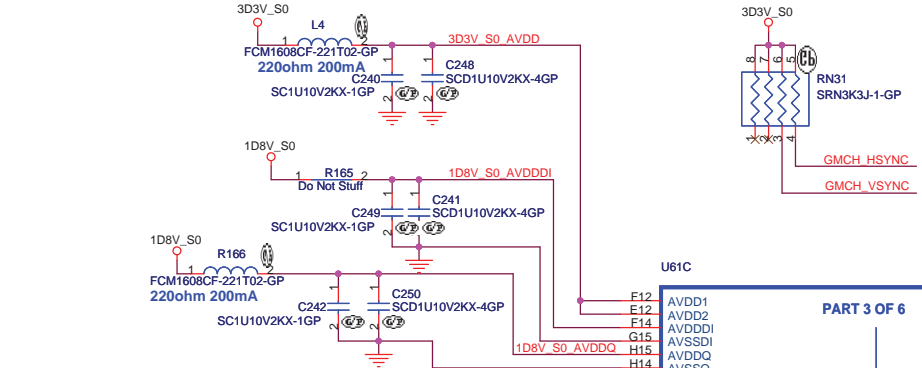
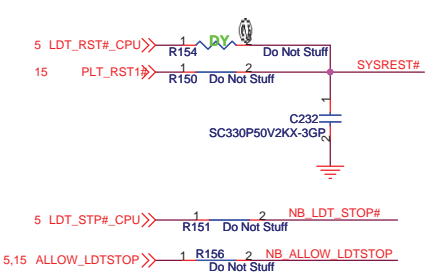


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ATI-RS780M_HT LINK&PCIE(1/3)

Size A3 Document Number **F7-GT** Rev -1

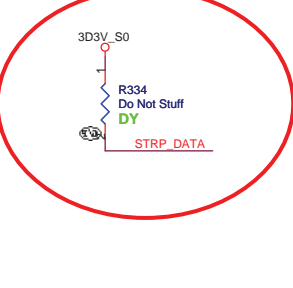
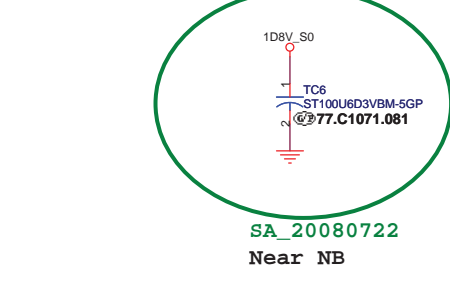
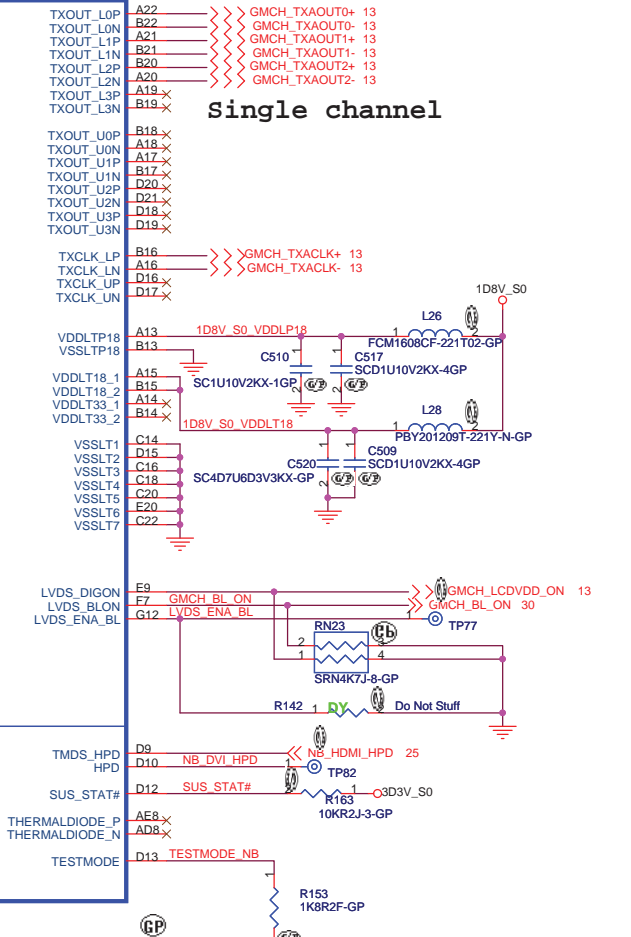
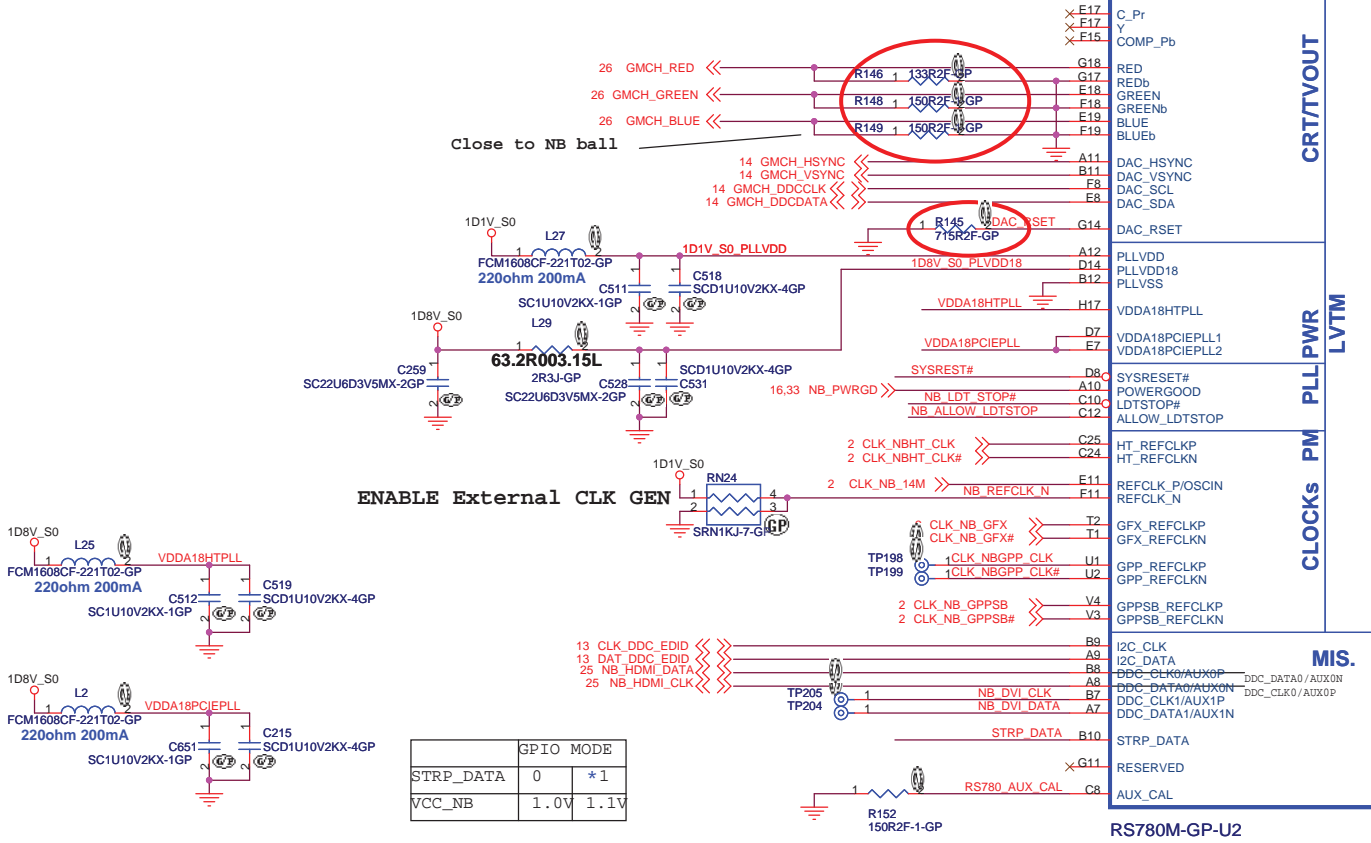
Date: Thursday, October 09, 2008 Sheet 10 of 47



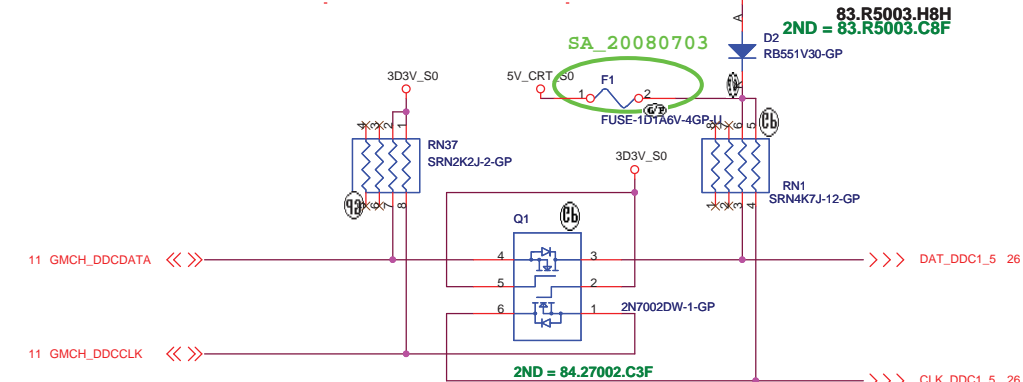
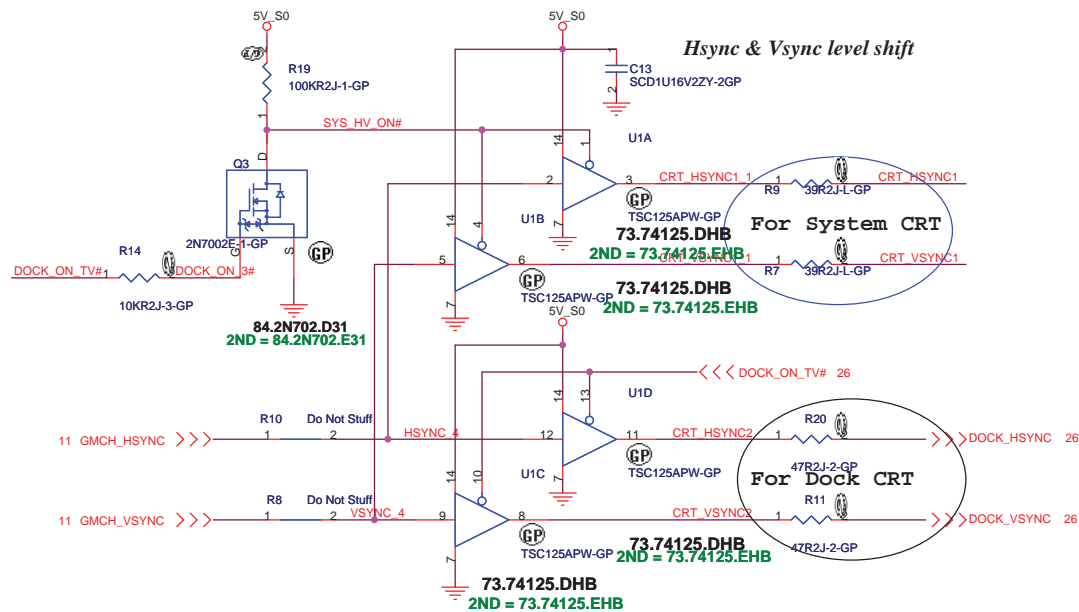
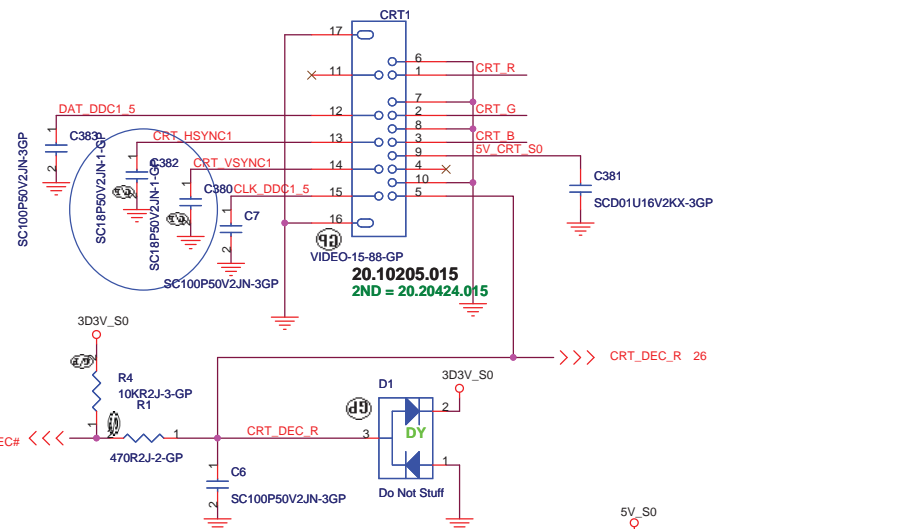
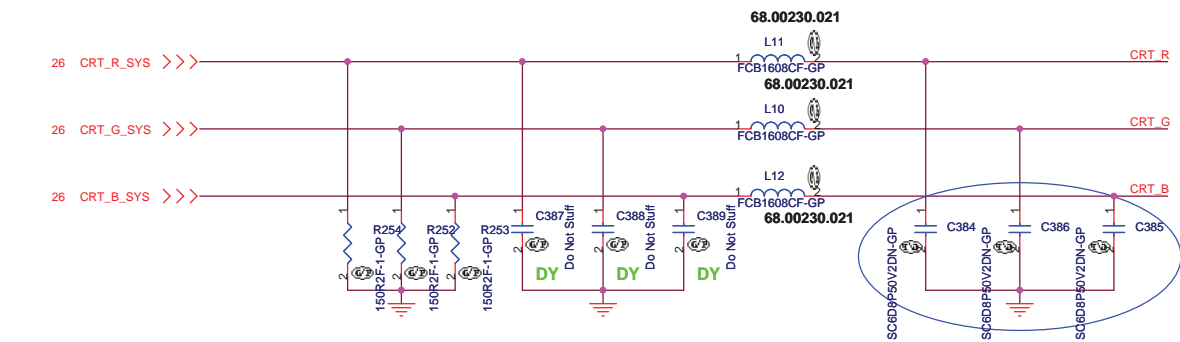
STRAP_DEBUG_BUS_GPIO_ENABLEb
 Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
 *1 :Disable 0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)
 *1 :Disable 0 : Enable

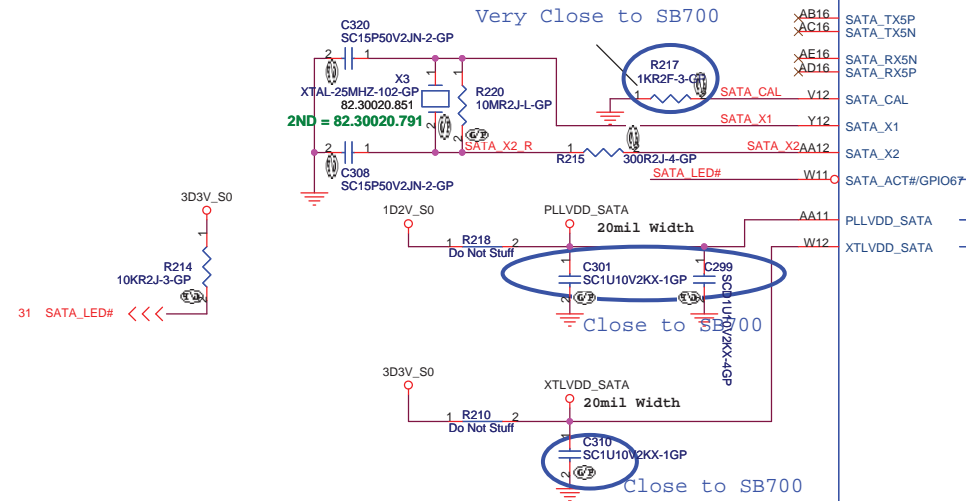
SUS_STAT#
 Selects Loading of STRAPS From EEPROM
 *1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected,
 or use default values if not connected



	GPIO MODE	
STRP_DATA	0	*1
VCC_NB	1.0V	1.1V

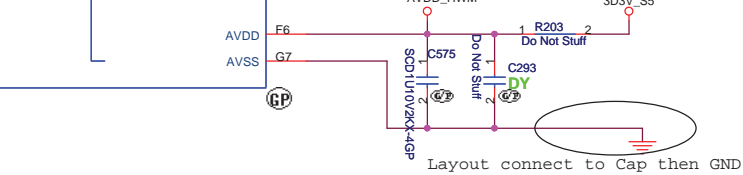
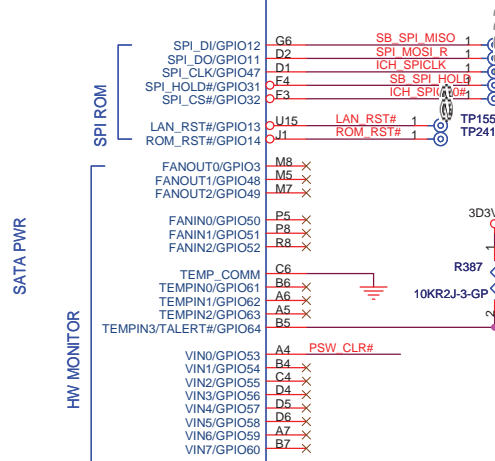
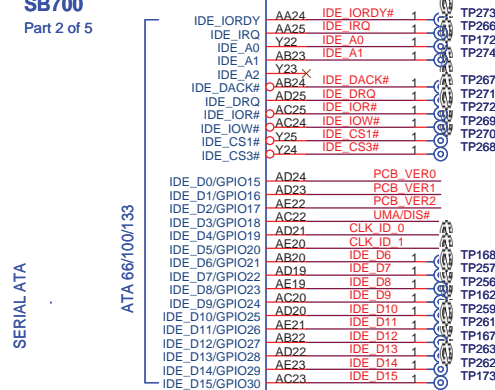


PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700

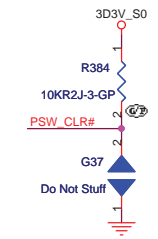
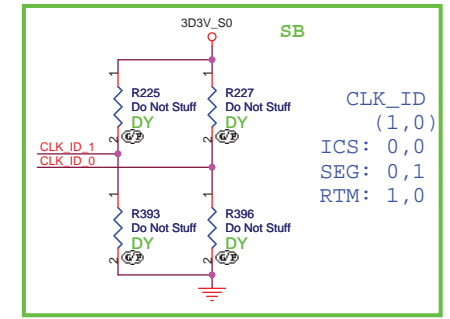
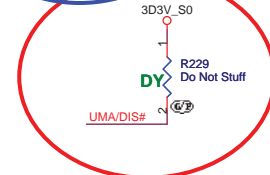
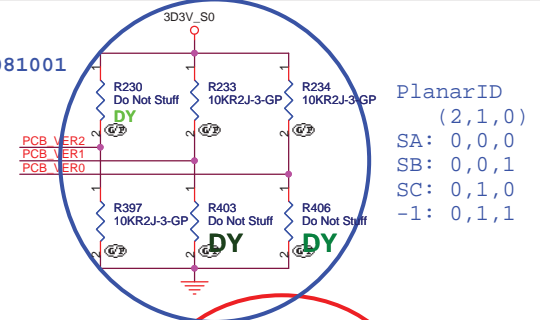


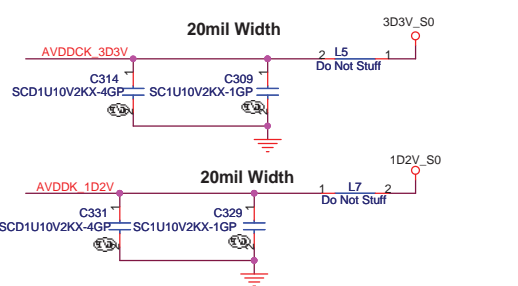
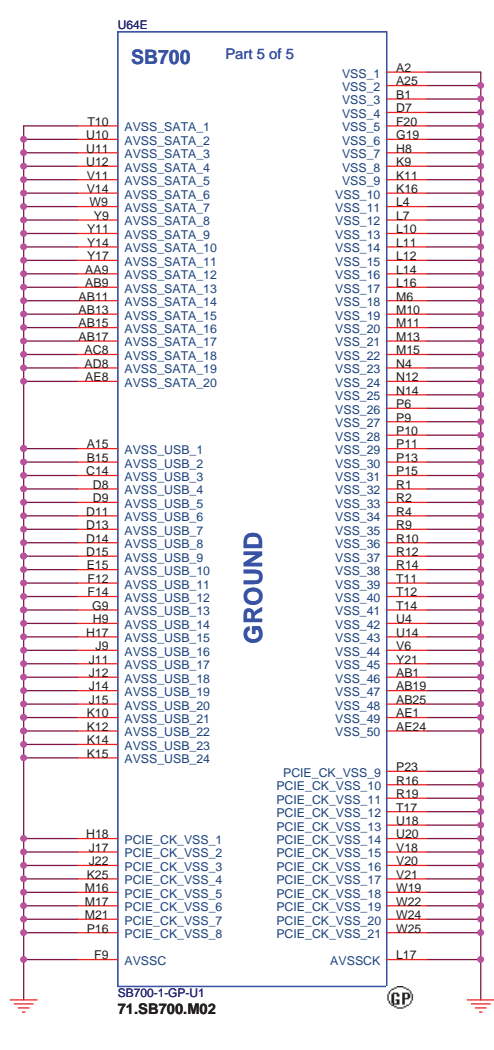
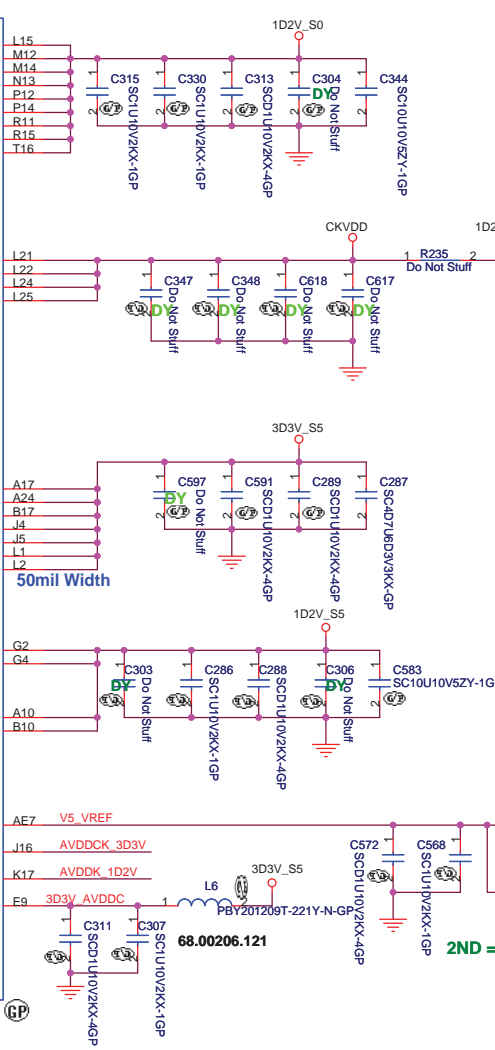
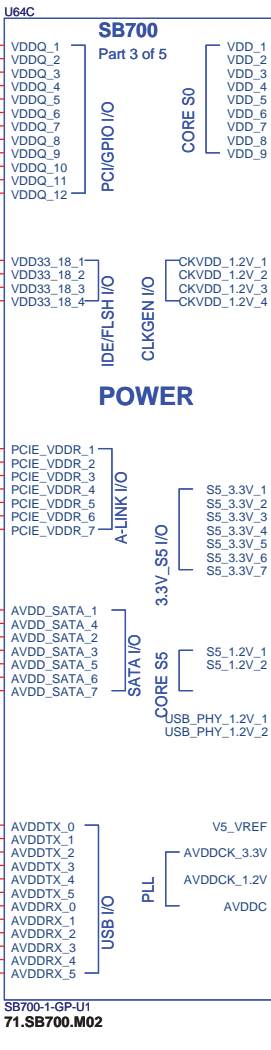
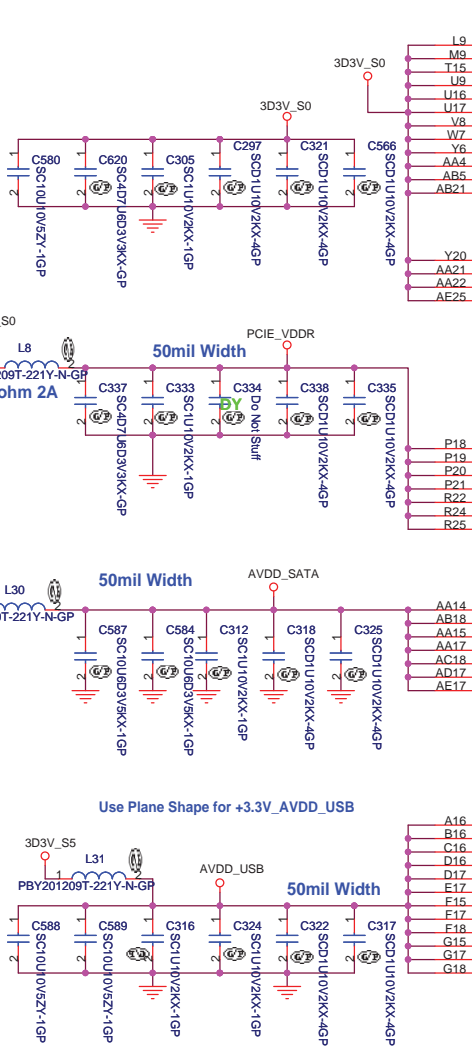
SB700

Part 2 of 5



-1_20081001





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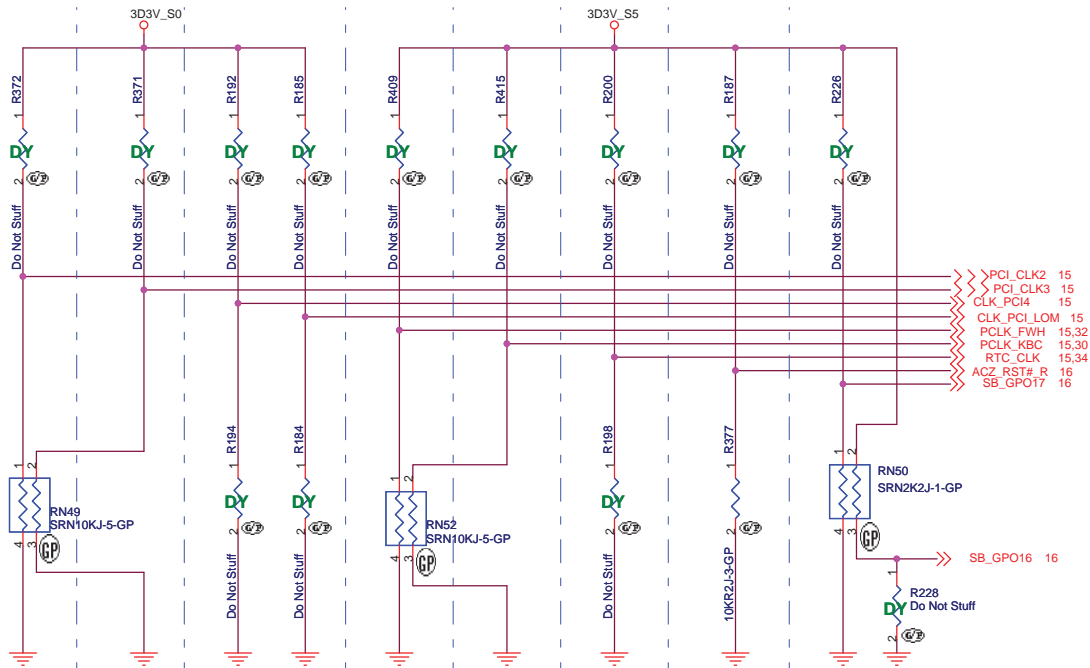
Title: ATi-SB700 POWER&GND (4/5)

Size: A3 Document Number: F7-GT Rev: -1

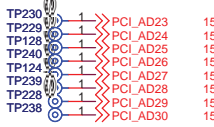
Date: Wednesday, October 01, 2008 Sheet: 18 of 47

REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



DEBUG STRAPS



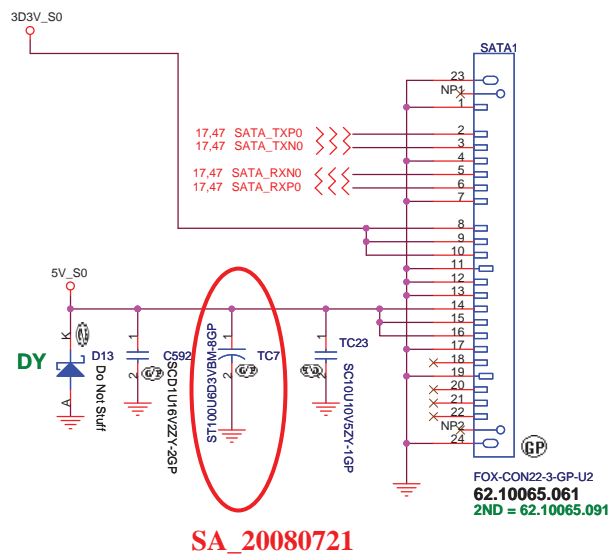
	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

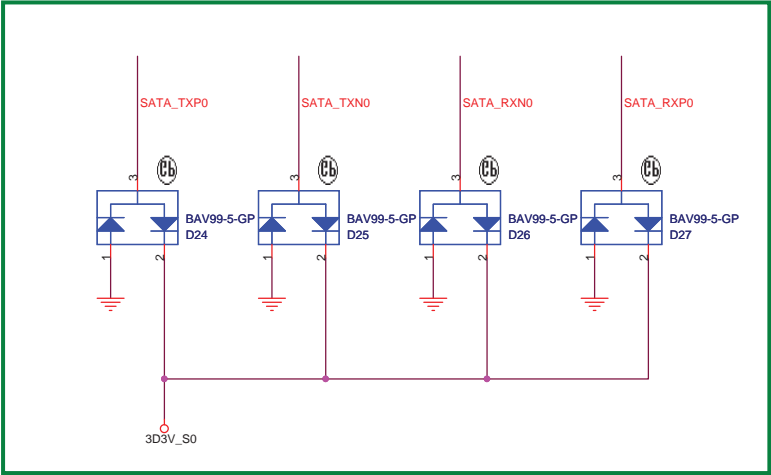
Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

SATA HDD Connector

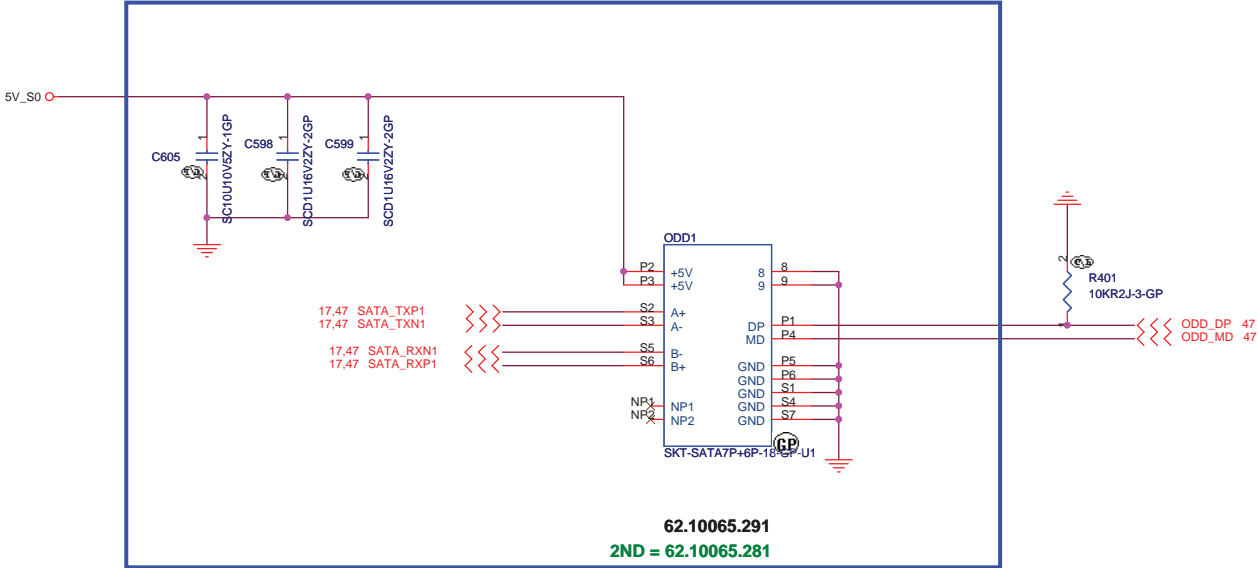


SA_20080721

For HDD

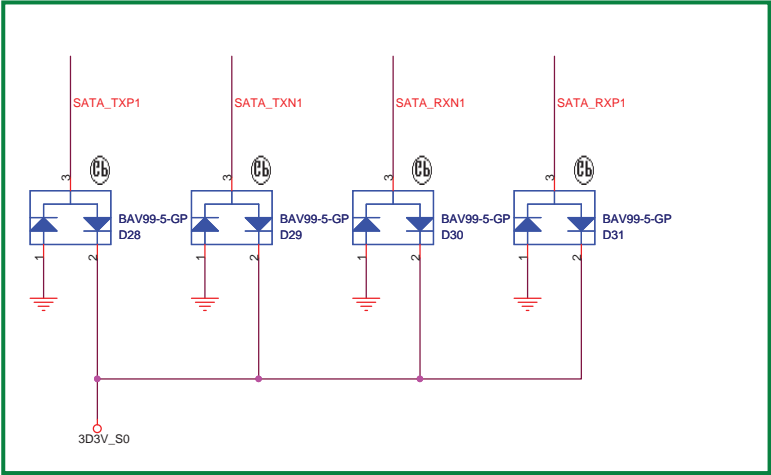


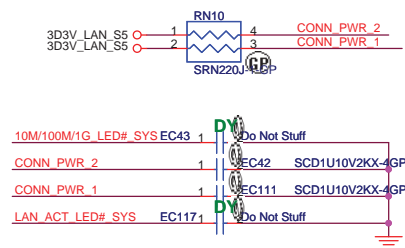
SA_20080714 SATA ODD Connector



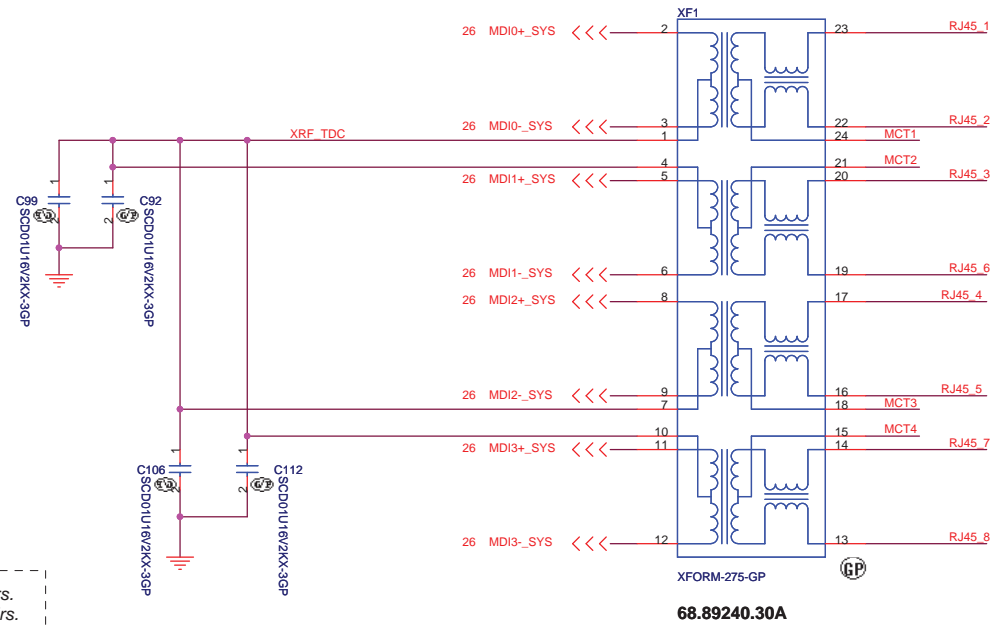
SB_20080825

For ODD



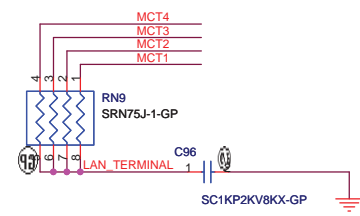


GIGA Lan Transformer

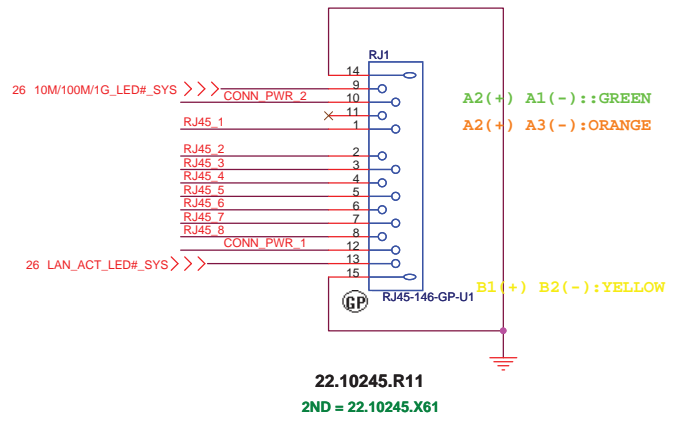


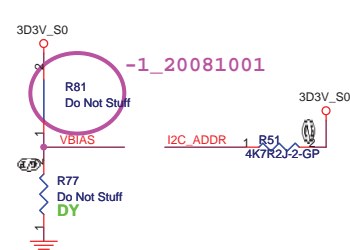
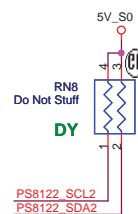
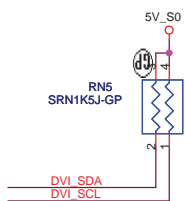
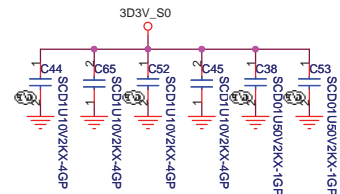
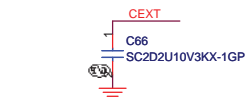
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



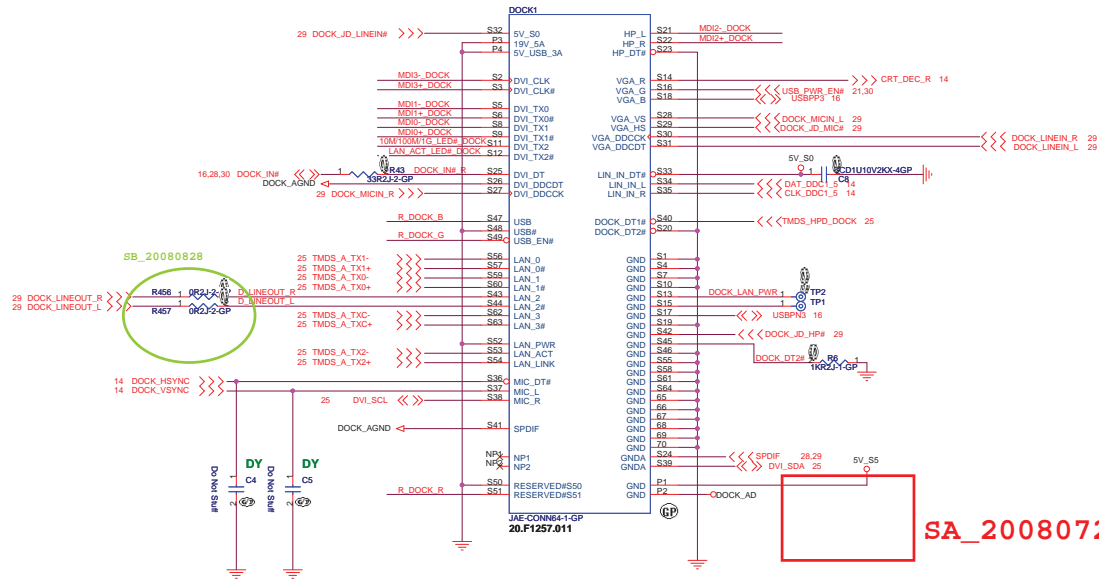
LAN Connector



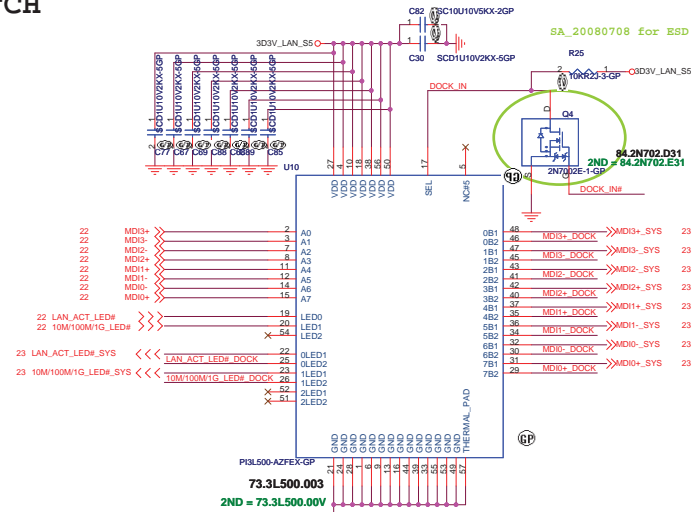


SA_20080709 change to Port Replicator

DOCK

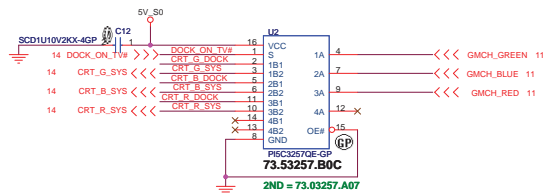
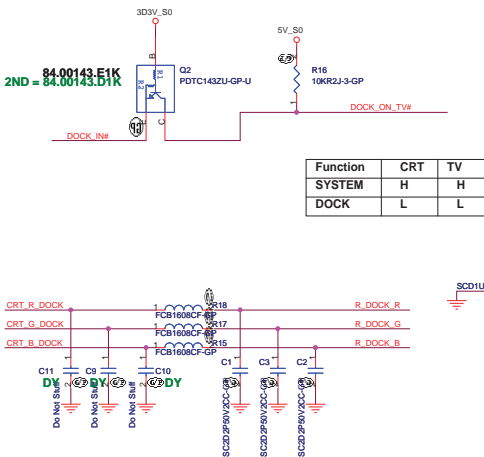


LAN SWITCH

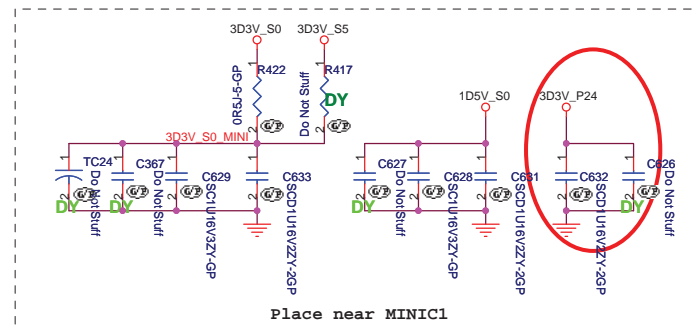
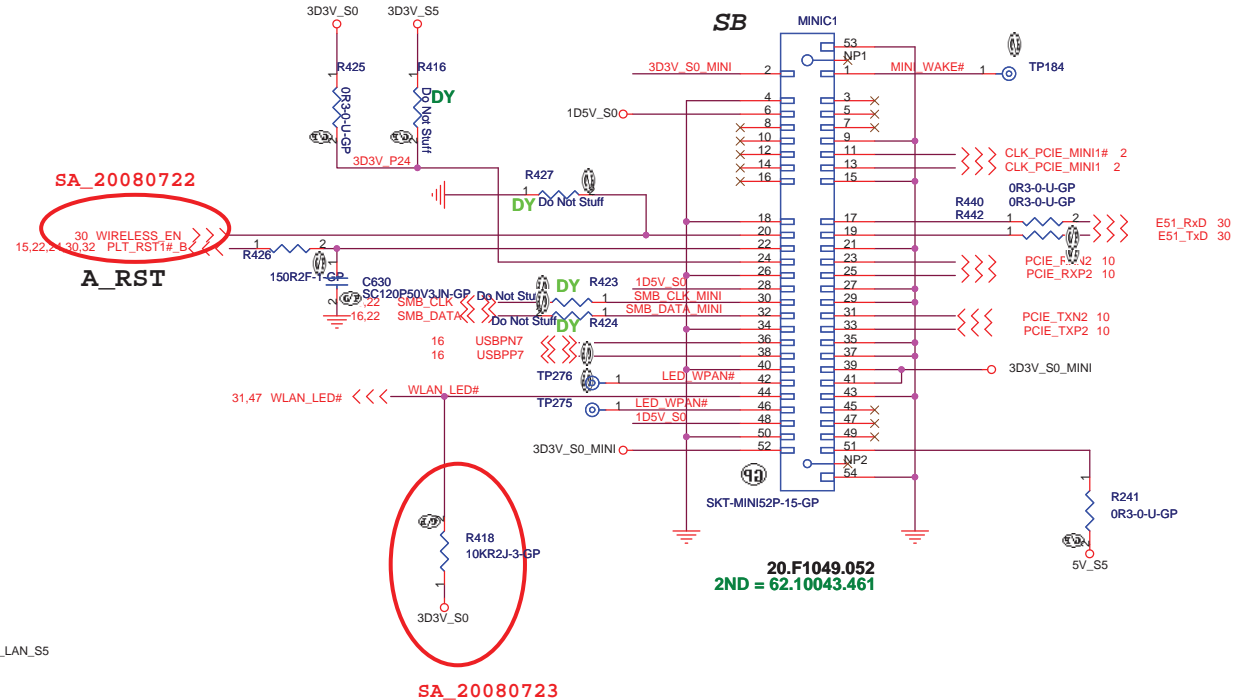


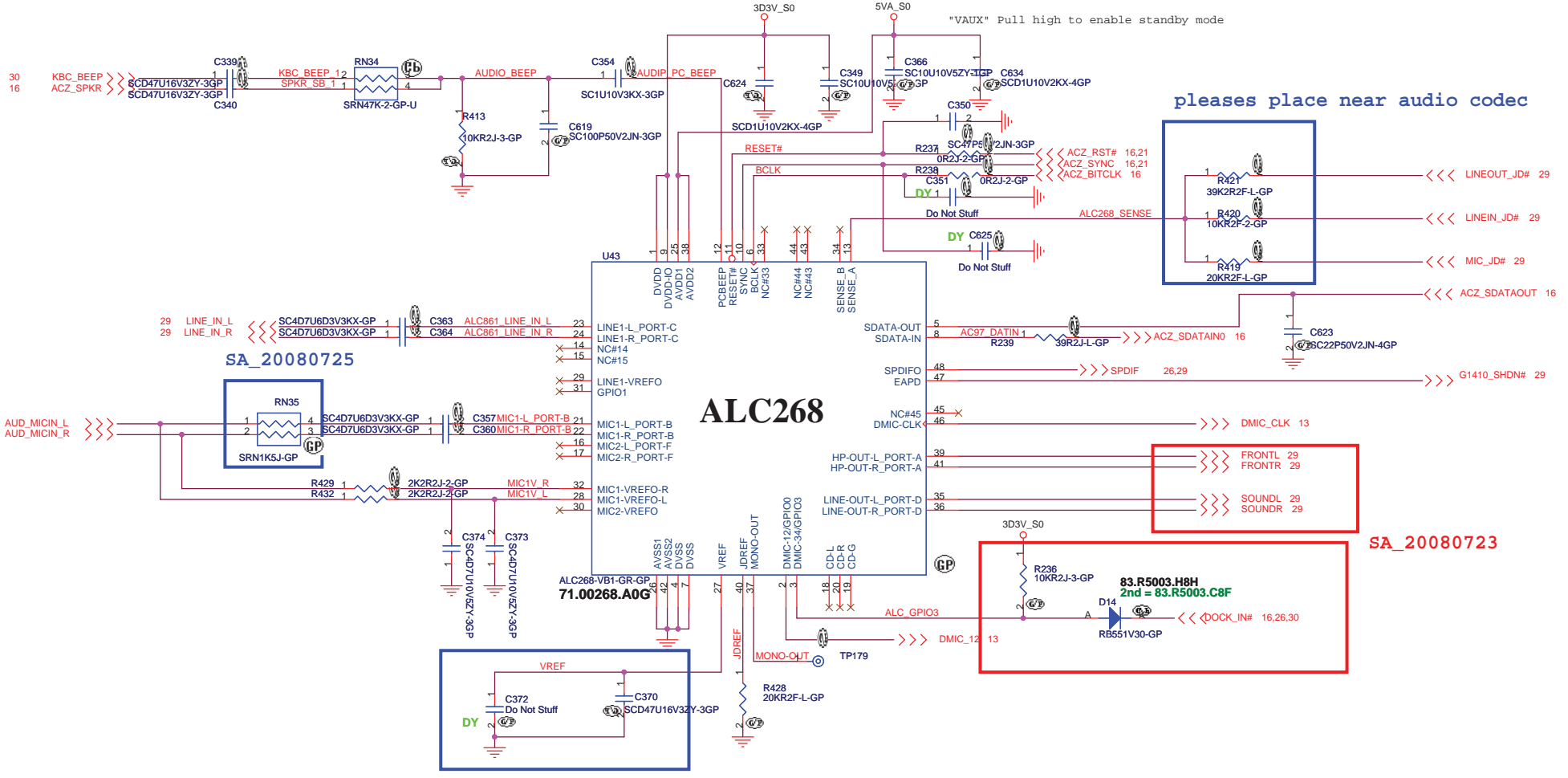
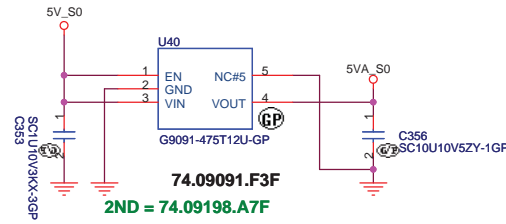
Function	LAN
SYSTEM	L
DOCK	H

CRT SWITCH



Mini Card Connector





pleases place near audio codec

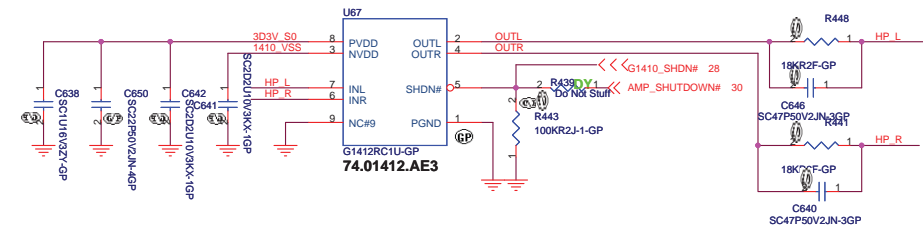
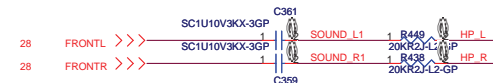
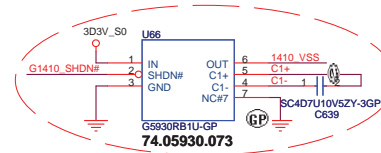
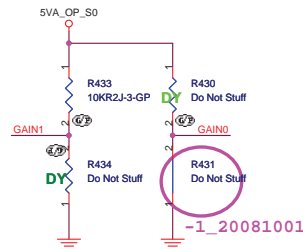
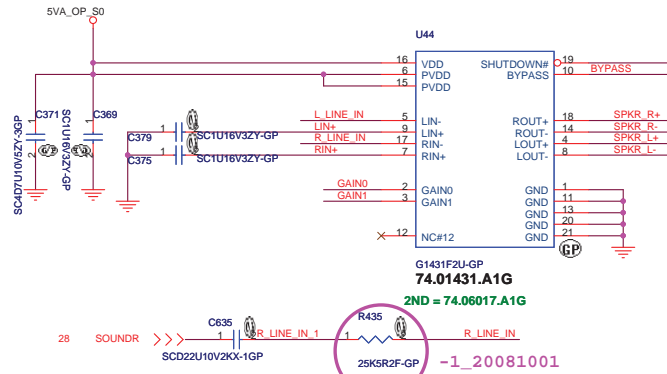
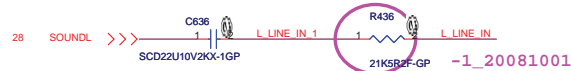
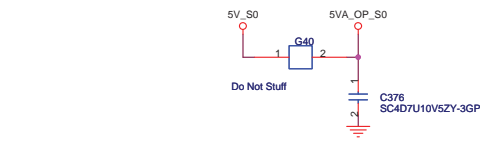
MP

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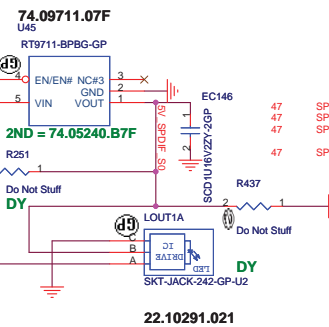
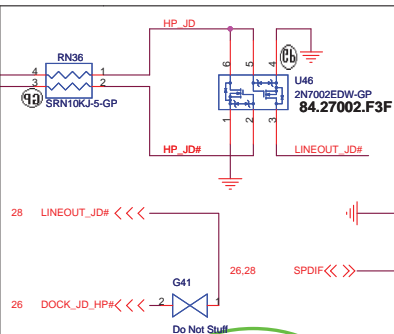
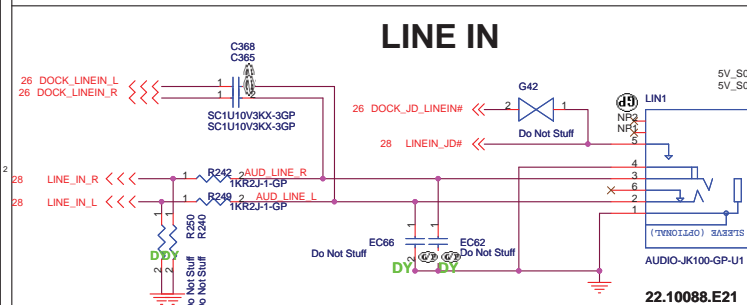
Title **AZALIA CODEC - ALC268**

Size Document Number **F7-GT** Rev **-1**

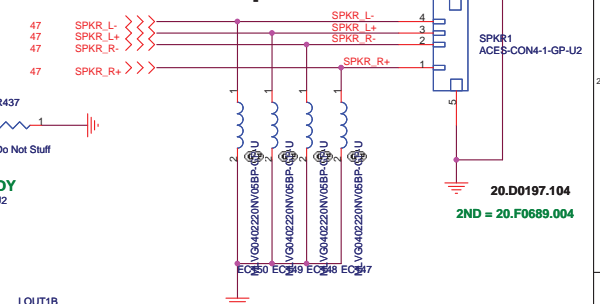
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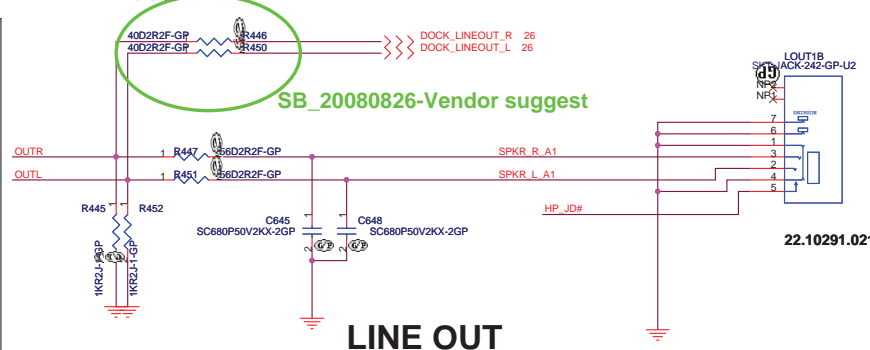
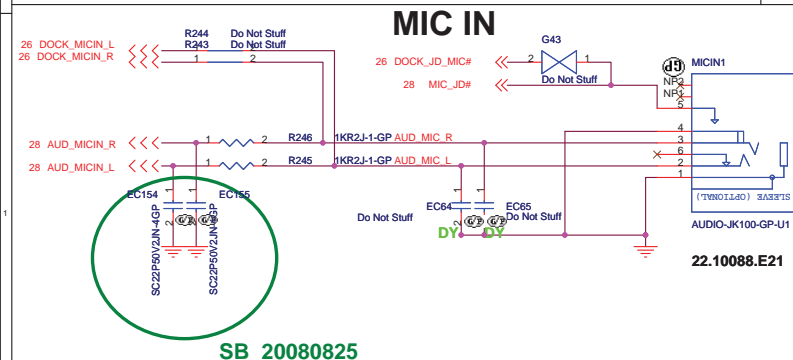
LINE IN



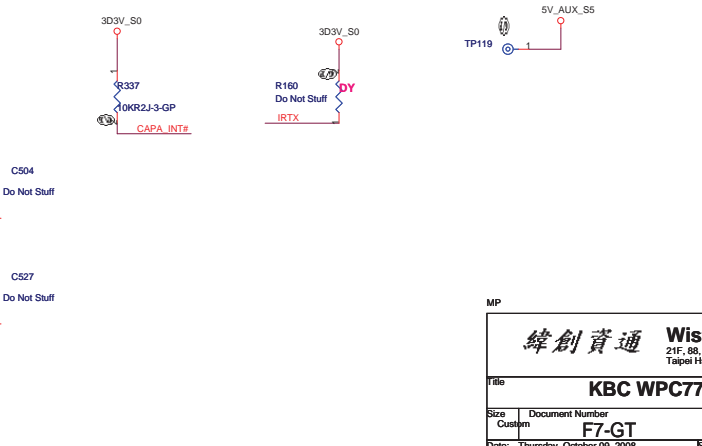
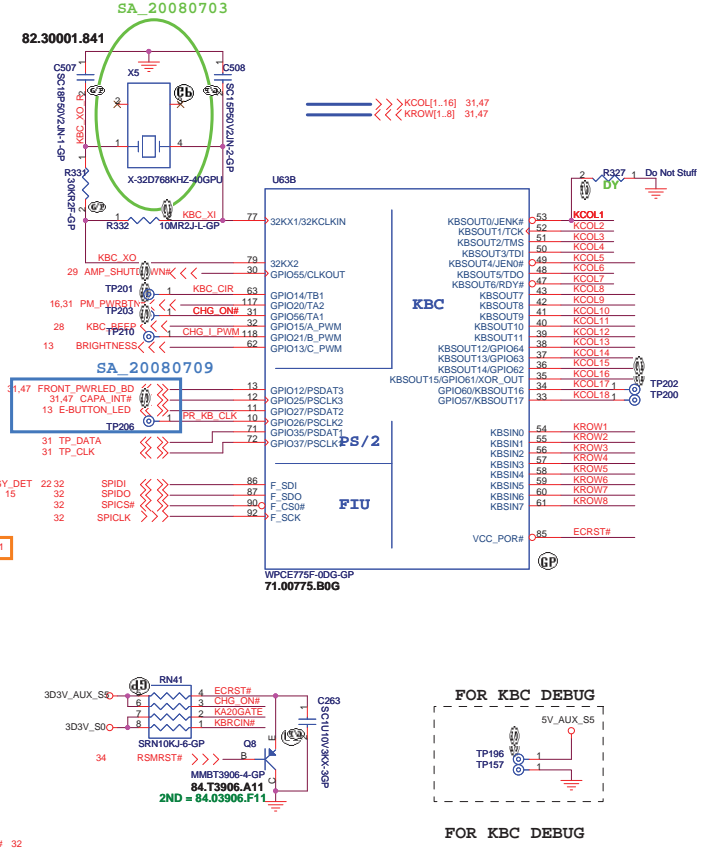
Internal Speaker



MIC IN



LINE OUT



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Title		KBC WPC773L	
Size	Document Number		Rev
Custom	F7-GT		-1
Date: Thursday, October 09, 2008		Sheet 30	of 47

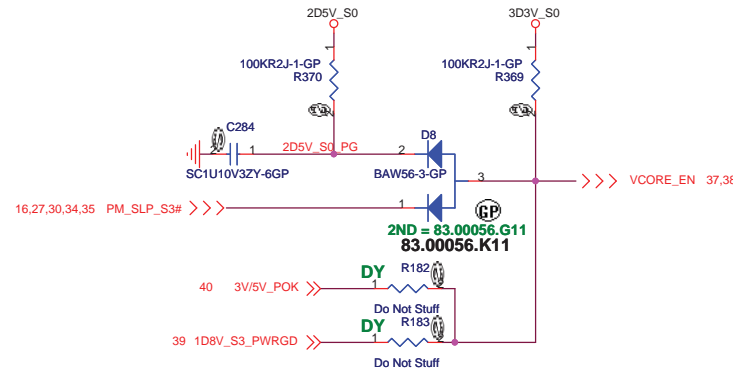
16M Bits



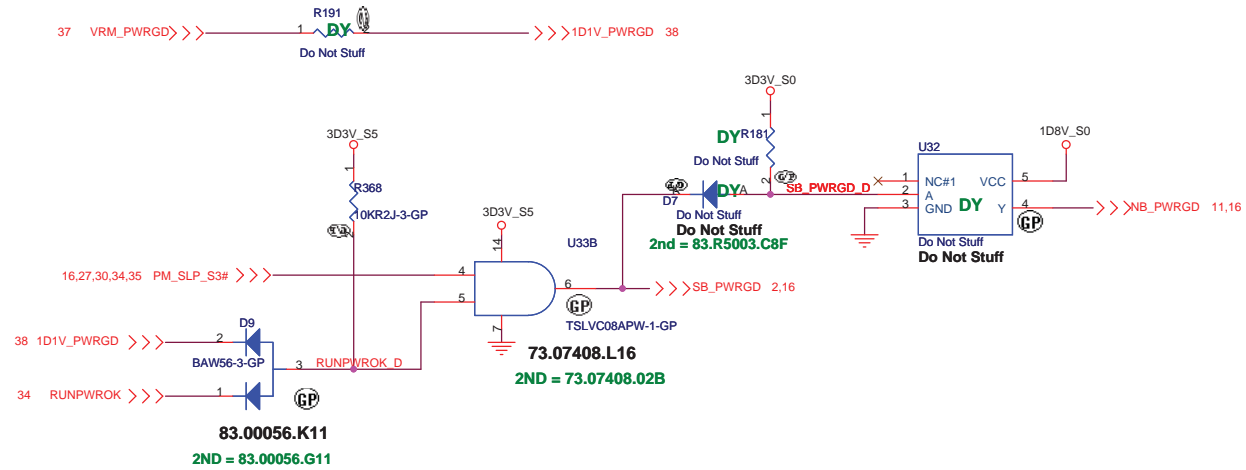
A15	(B1)
A14	(B2)
\vdots	\vdots
A2	(B14)
A1	(B15)

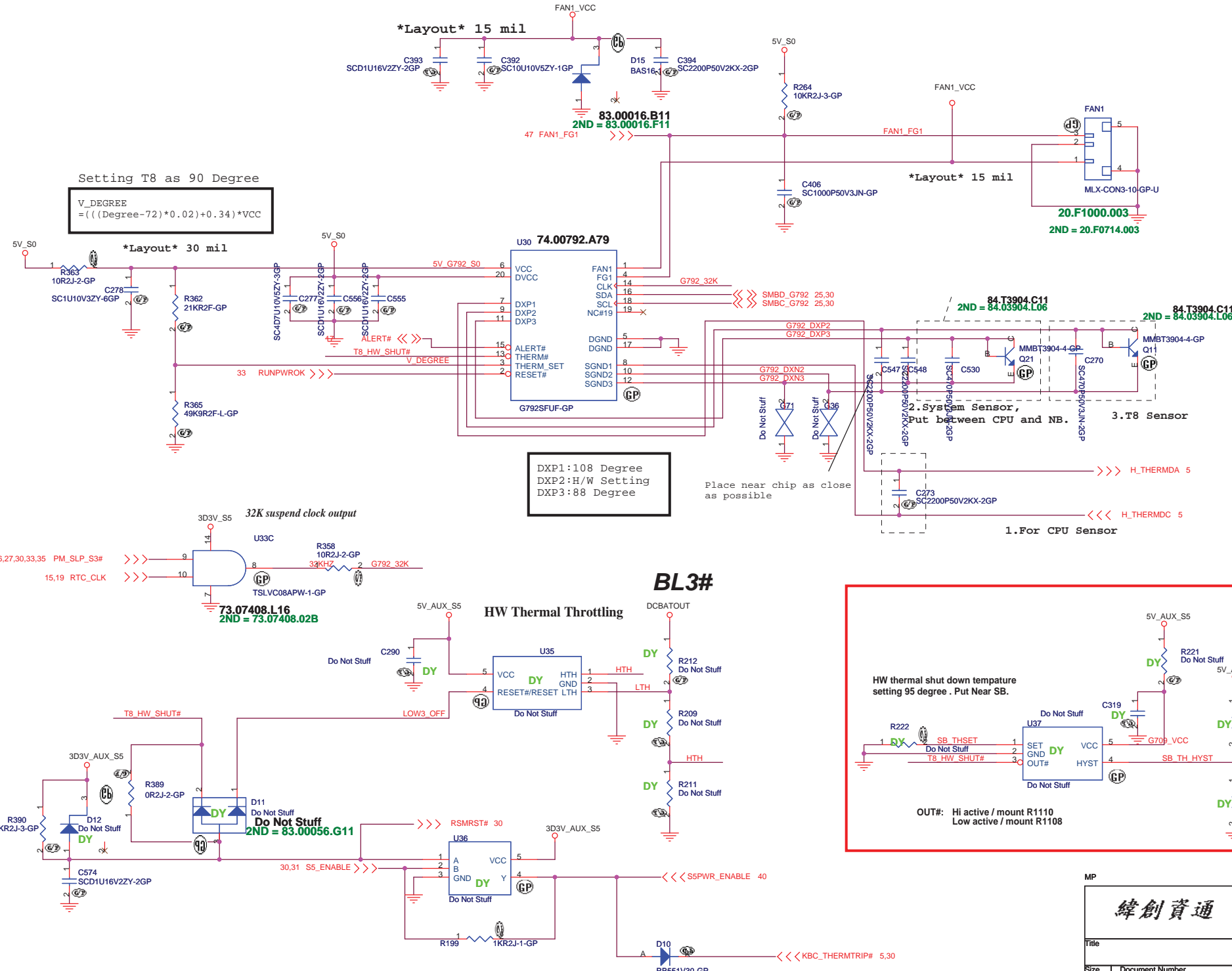
The diagram illustrates the Golden Finger connector for a debug board. It features a central U39 chip with 15 pins (A1-A15 on the left, B1-B15 on the right). The connections are as follows:

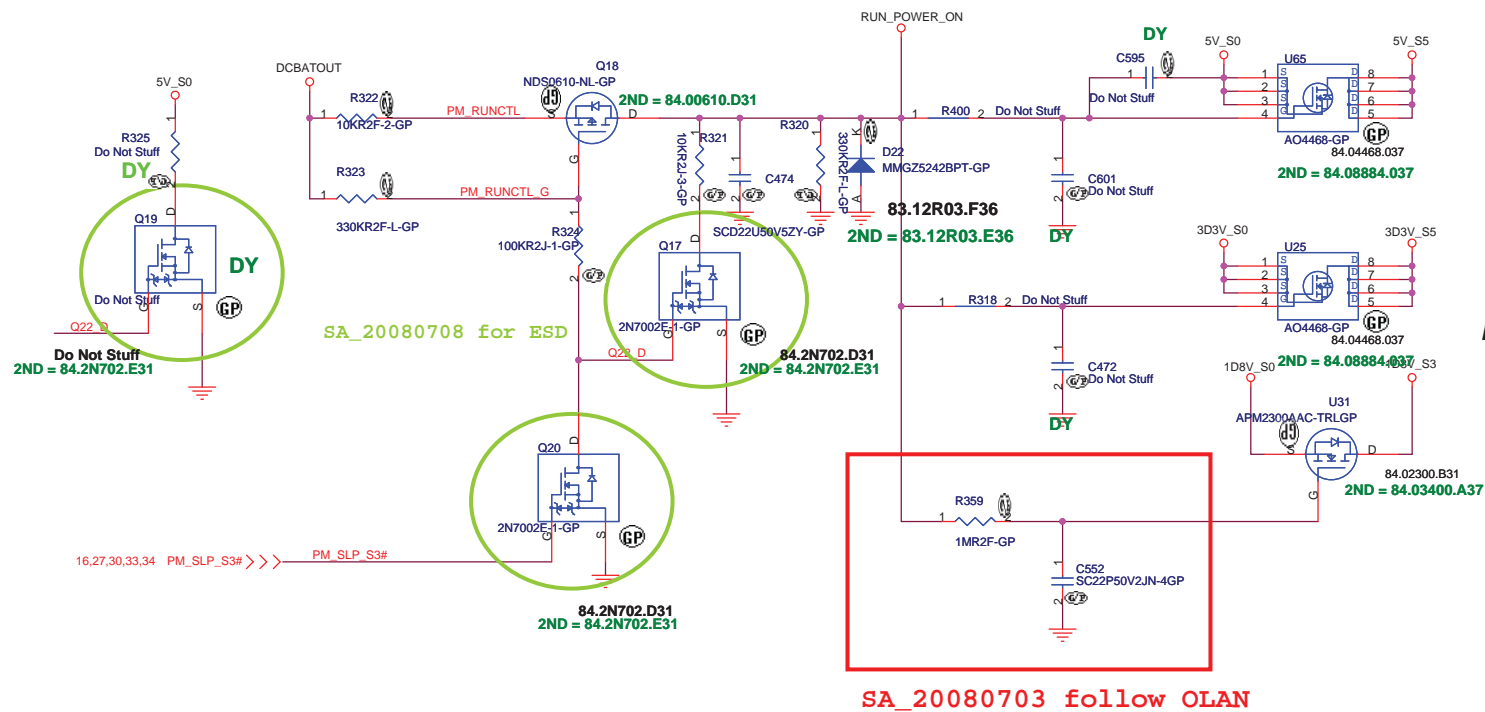
- Power and Ground:**
 - 5V_S0 is connected to A1 and B1.
 - 3D3V_S0 is connected to A7 and B7.
 - 3D3V_S0 is connected to A15 and B15.
 - Ground is connected to A15 and B15.
- Control and Data Signals:**
 - A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15 are connected to the left side of the U39 chip.
 - B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15 are connected to the right side of the U39 chip.
 - PLC_RST1#_B is connected to B1.
 - LPC_DFRAME# is connected to B2.
 - PLCK_FWH# is connected to B3.
 - LPC_LAD3 is connected to B8.
 - LPC_LAD2 is connected to B9.
 - LPC_LAD1 is connected to B10.
 - LPC_LAD0 is connected to B11.
 - EXT_FWH# is connected to B12.
 - 3D3V_S0 is connected to B7.
- Other Connections:**
 - SA_20080722 is connected to A1 and B1.
 - SA_20080722 is connected to B1 and B2.
 - SA_20080722 is connected to B2 and B3.
 - SA_20080722 is connected to B3 and B4.
 - SA_20080722 is connected to B4 and B5.
 - SA_20080722 is connected to B5 and B6.
 - SA_20080722 is connected to B6 and B7.
 - SA_20080722 is connected to B7 and B8.
 - SA_20080722 is connected to B8 and B9.
 - SA_20080722 is connected to B9 and B10.
 - SA_20080722 is connected to B10 and B11.
 - SA_20080722 is connected to B11 and B12.
 - SA_20080722 is connected to B12 and B13.
 - SA_20080722 is connected to B13 and B14.
 - SA_20080722 is connected to B14 and B15.



P/H @ 1D8V_S3 PAGE



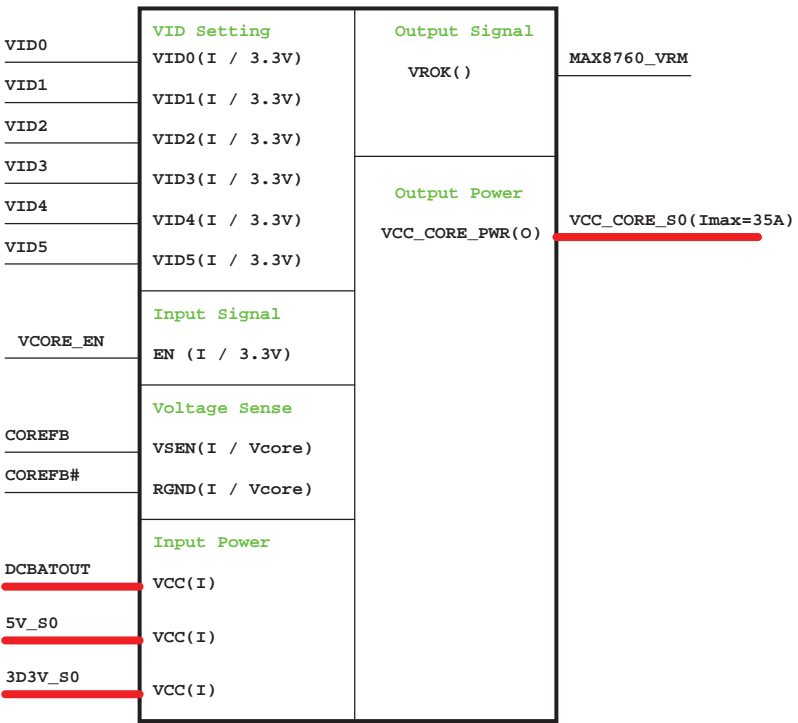




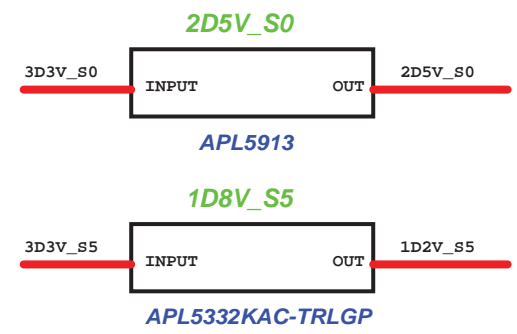
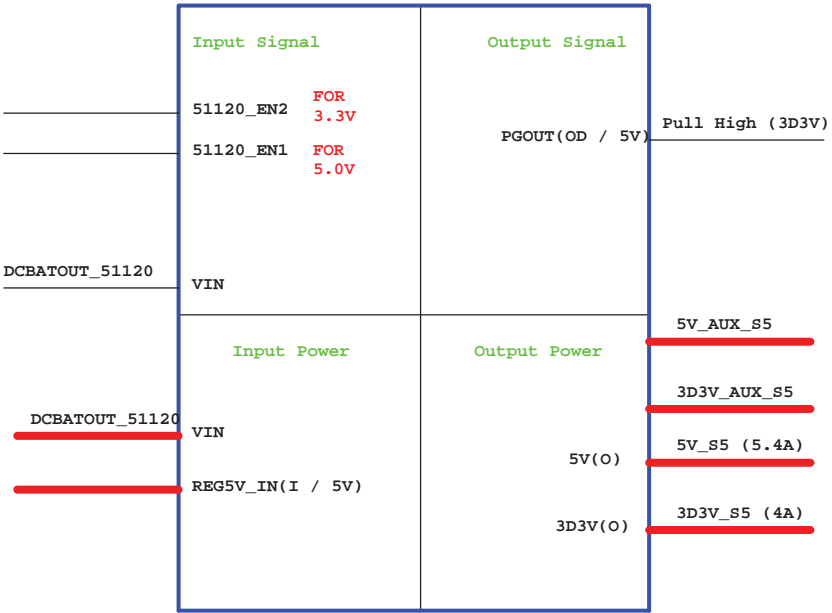
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Title			
PWR CTL LOGIC / PWR PLANE			
Size	Document Number	Rev	
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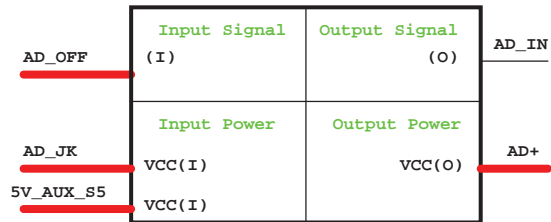
CPU_CORE
ISL6264CRZ



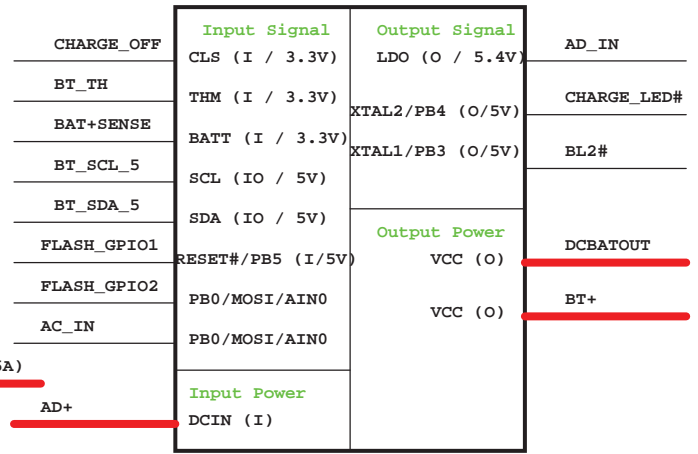
TI TPS51120
3D3V/5V



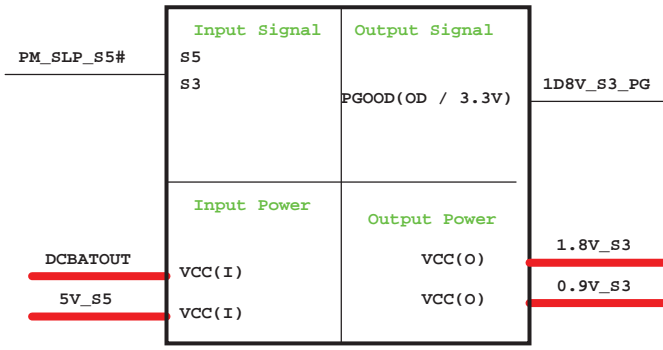
Adapter



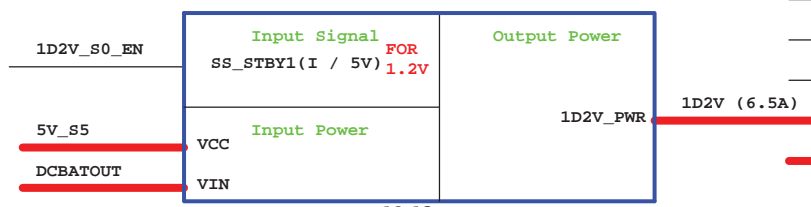
Charger_ISL6255



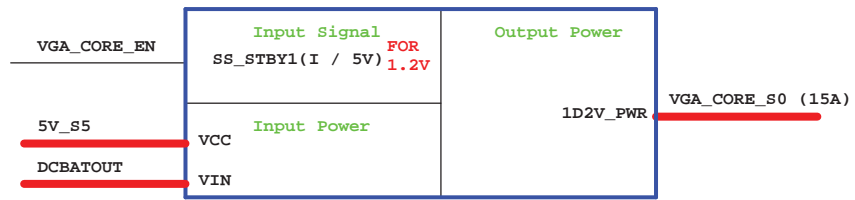
TI TPS51116
1.8V / 0.9V



ISL6268_1D2V



ISL6268_VGA_CORE



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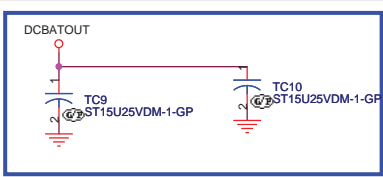
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Power Block Diagram

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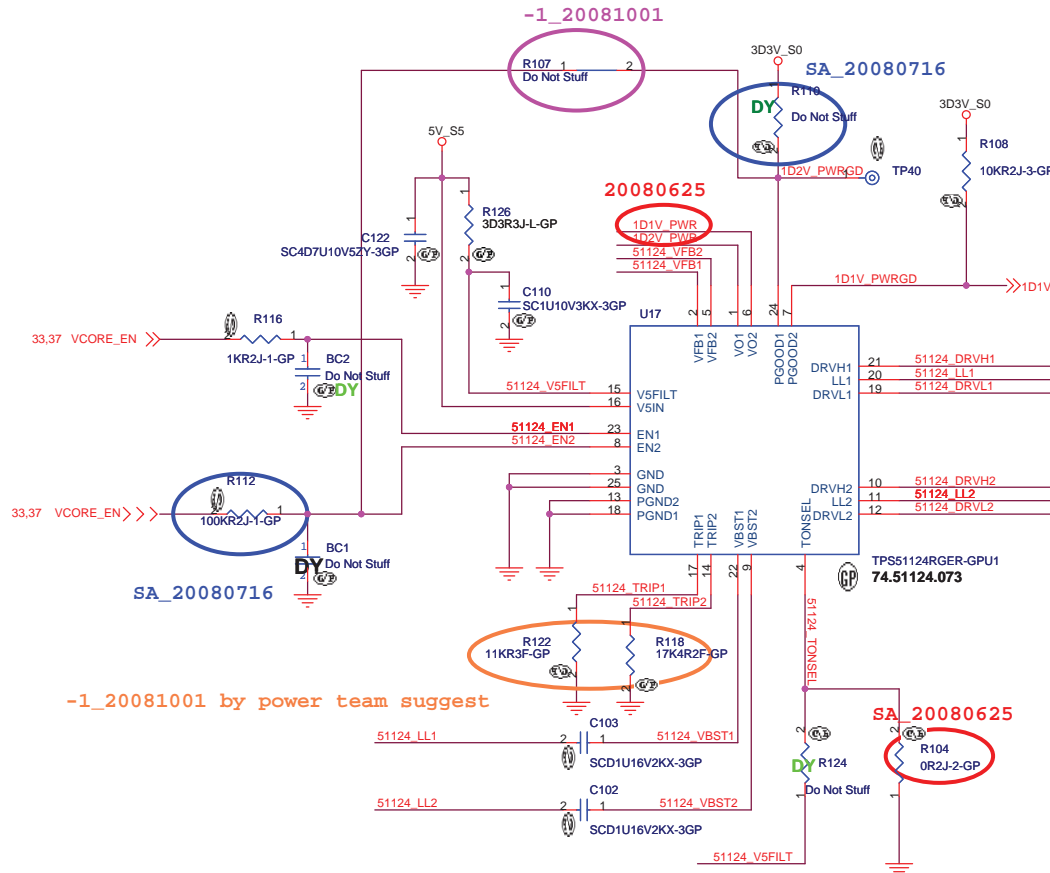
Rev -1



SB_20080827

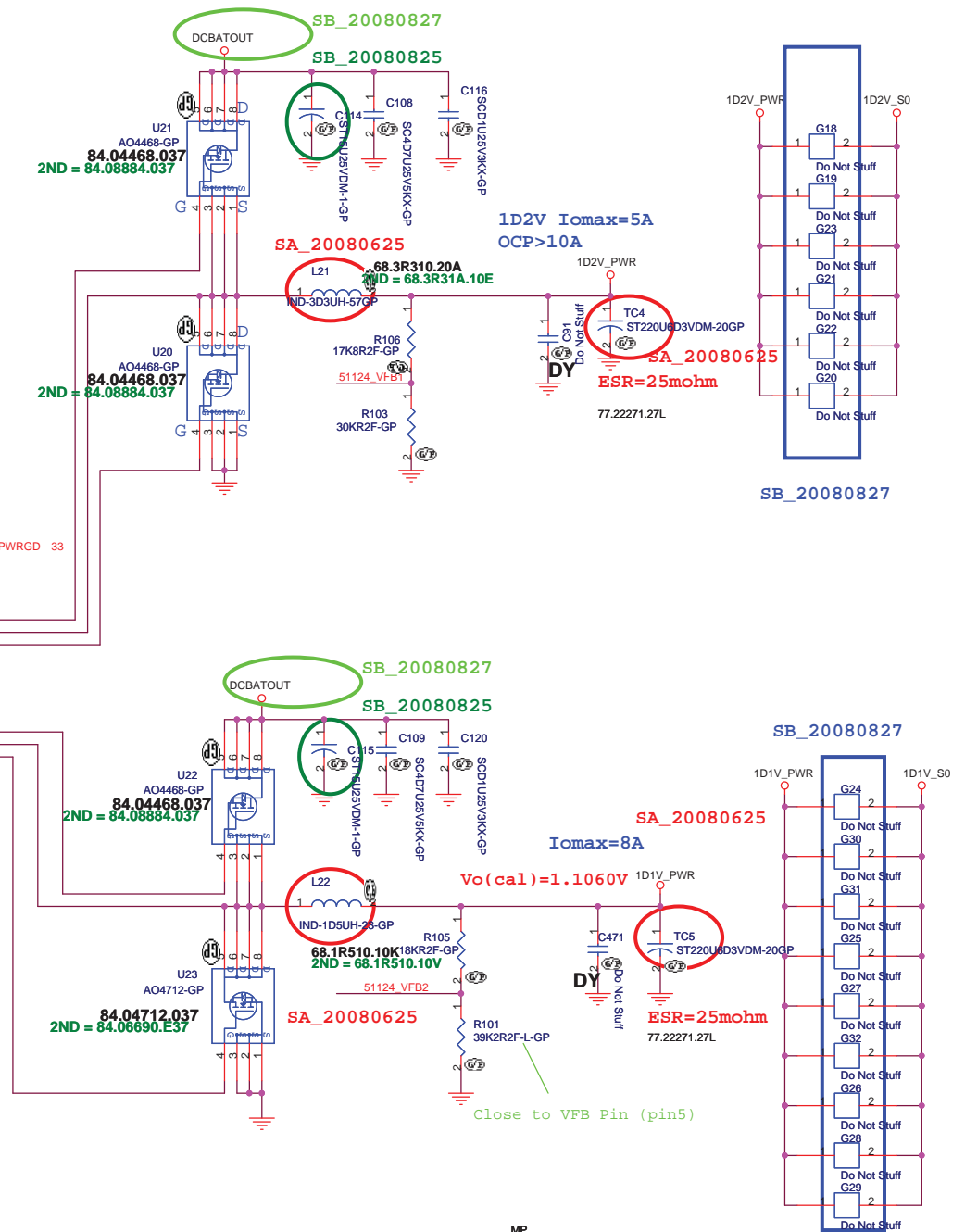
$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in}))$$



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1+R2)/R2$ ---> PWM mode
 $V_{out} = 0.764V * (R1+R2)/R2$ ---> Skip Mode

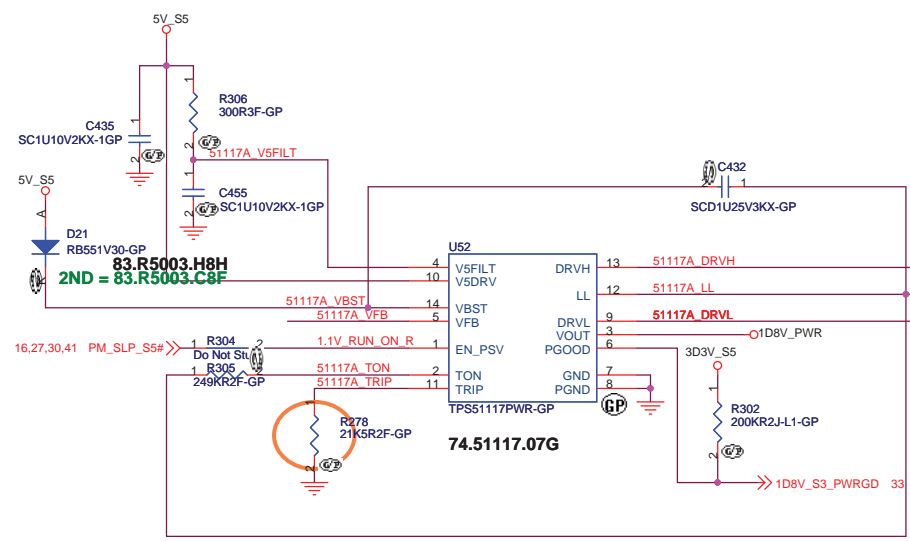


MP

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Title: TPS51124 1D1V 1D2V

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-1_20081001 by power team suggest

84.04468.037
2ND = 84.08884.037

84.04706.037

Cyntec 10*10*4
DCR=4.2mohm, Irating=16A
Isat=33A

SB_20080827

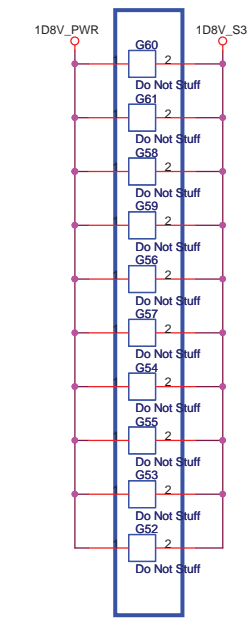
Vo(cal)=1.8214V

1D8V Iomax=10A
OCP>15A

ESR=1.5mohm
2ND = 77.C3371.10L
77.23371.L01

$V_{out} = 0.75 * (R1 + R2) / R2$

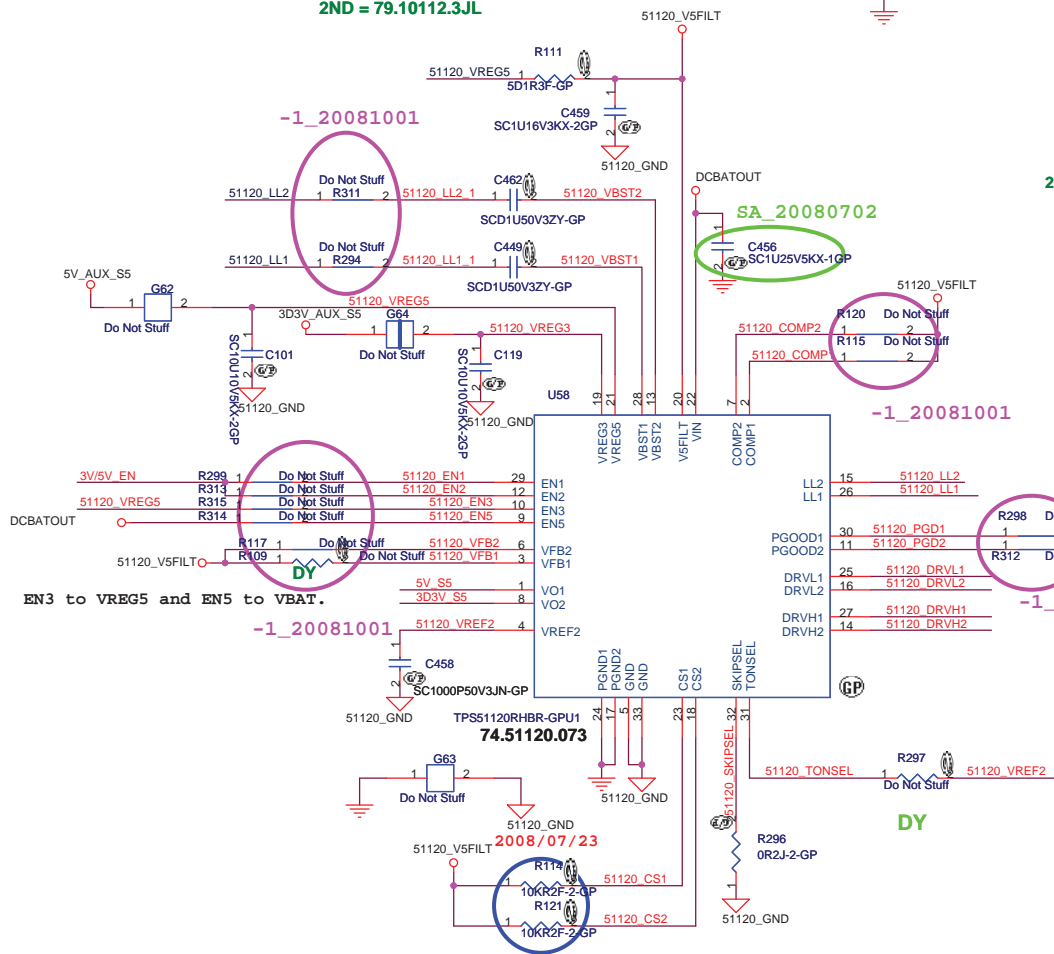
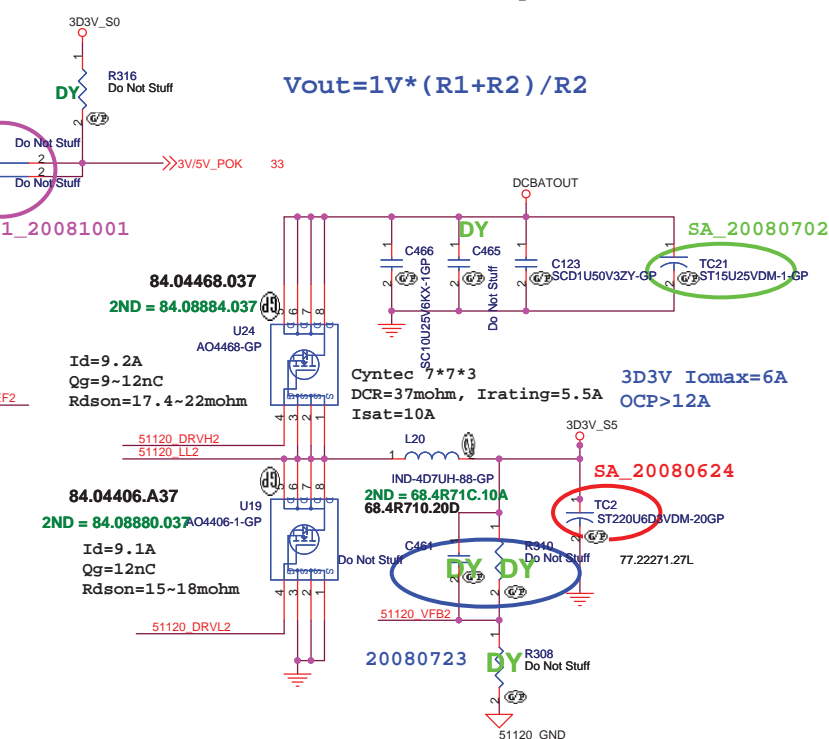
-1_20081001 by power team suggest



SB_20080827

MP

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Title	
1D8V(TPS5117)	
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	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	switcher OFF	not use	Swither ON	Switcher ON

For TPS51120,
Vout=5V

1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
 2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
 3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
 Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
 2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
 3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

M

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Title

TPS51120 5V 3D3VSize
A3

Document Number

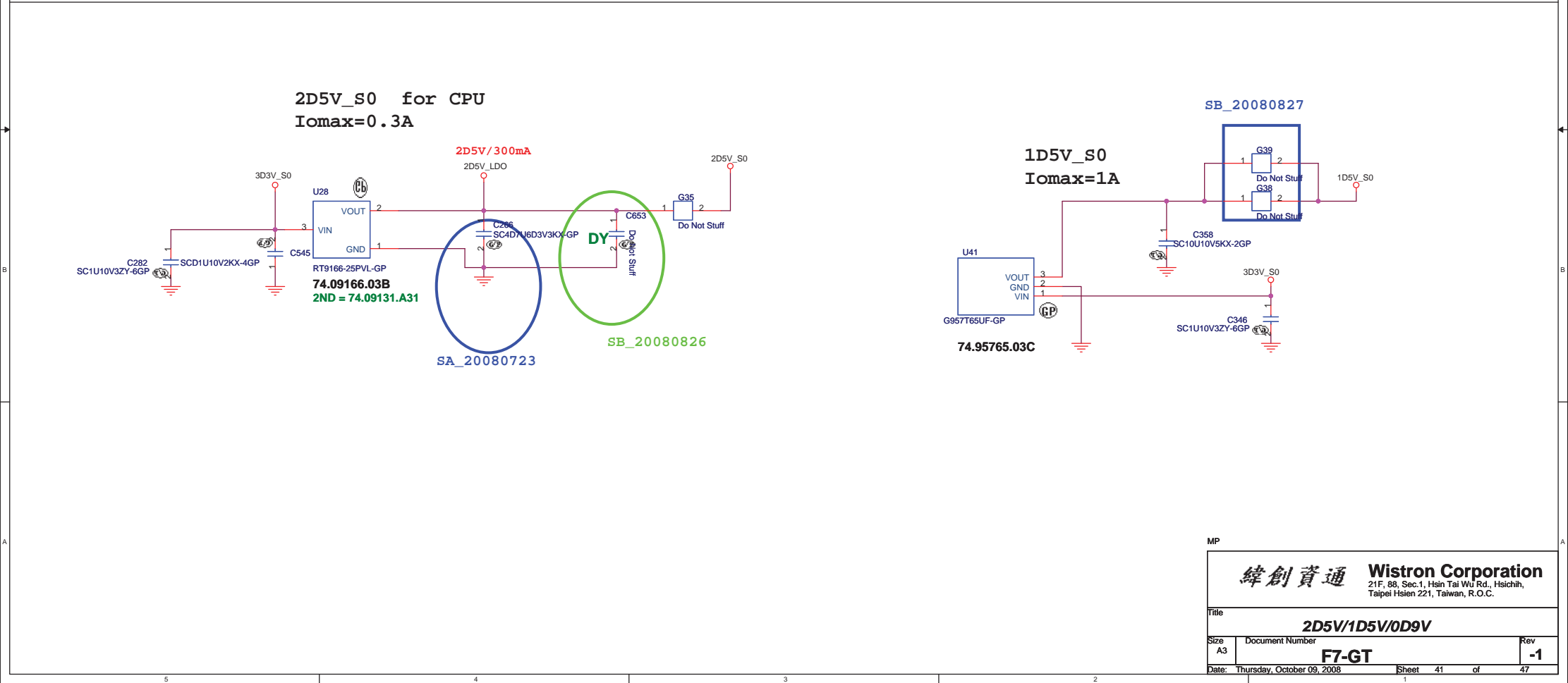
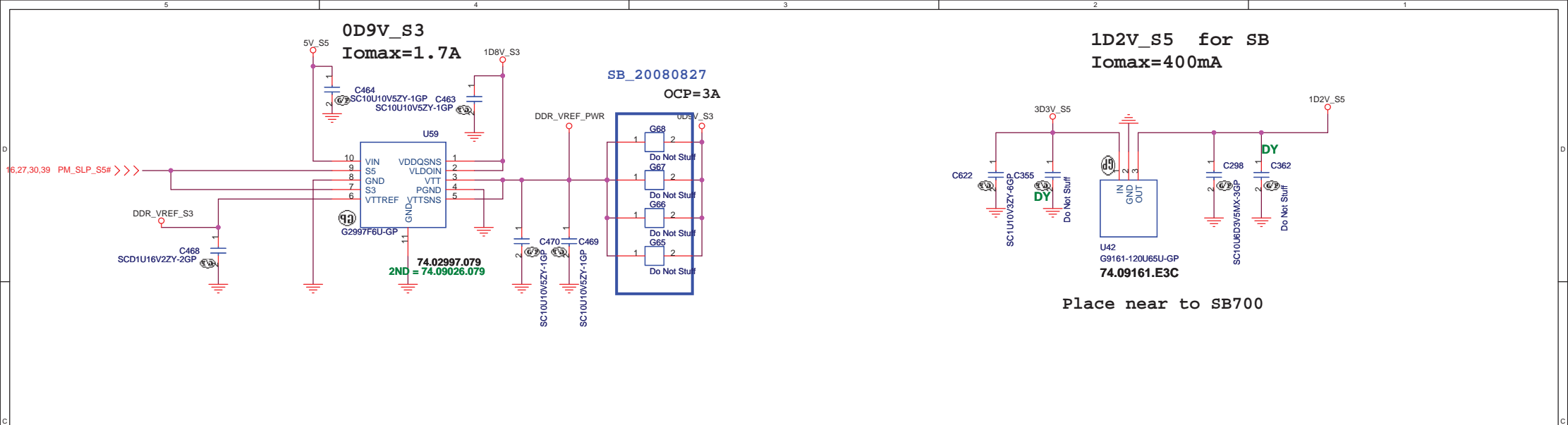
F7-GT

Rev

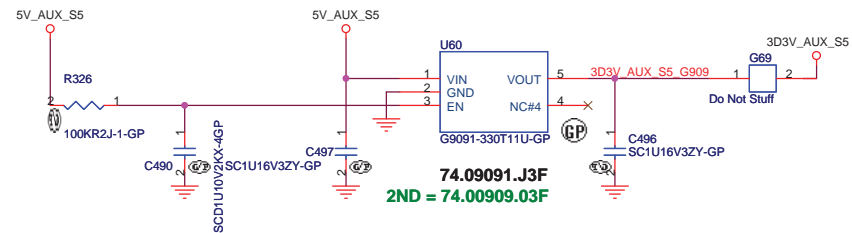
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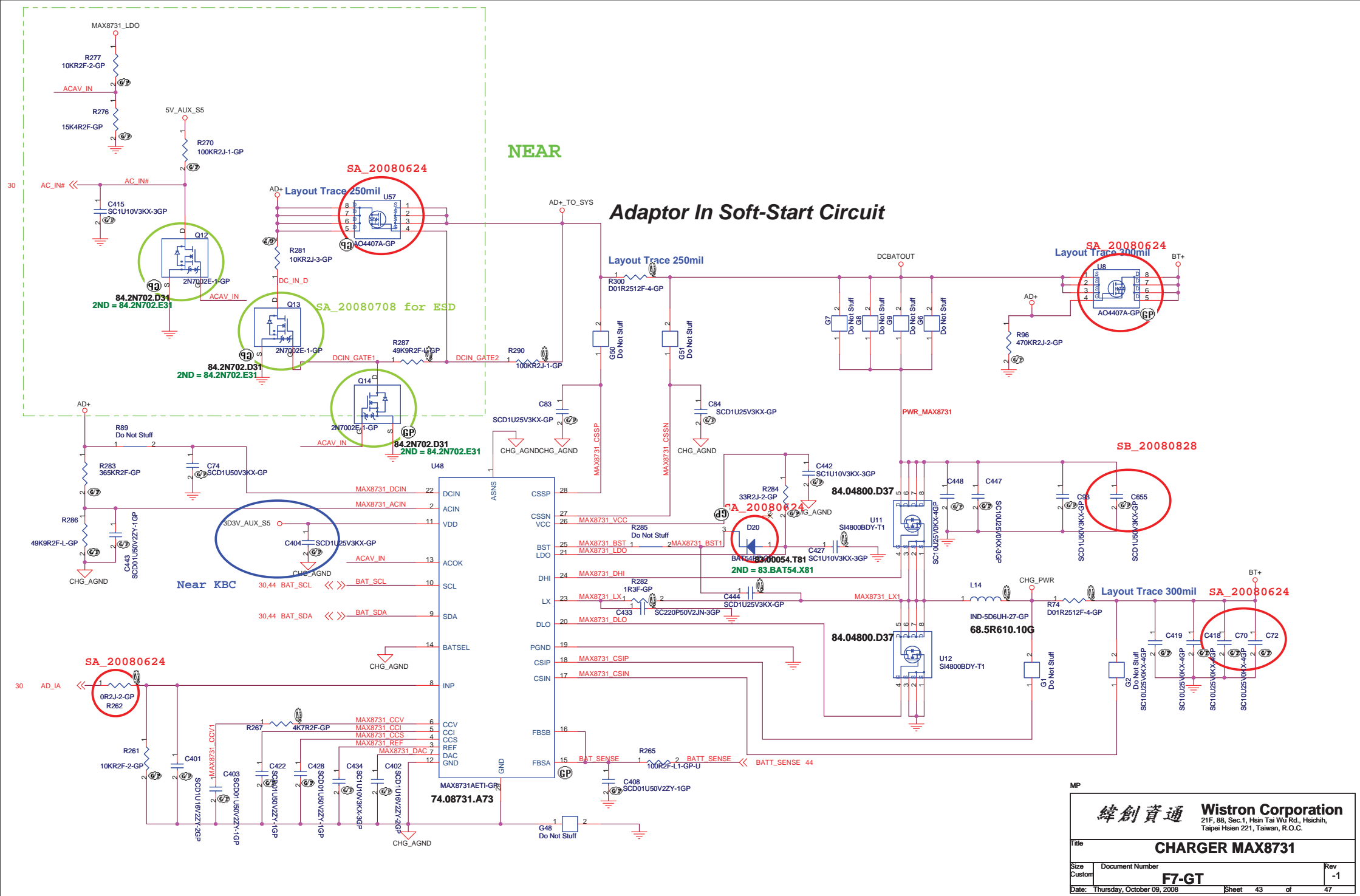
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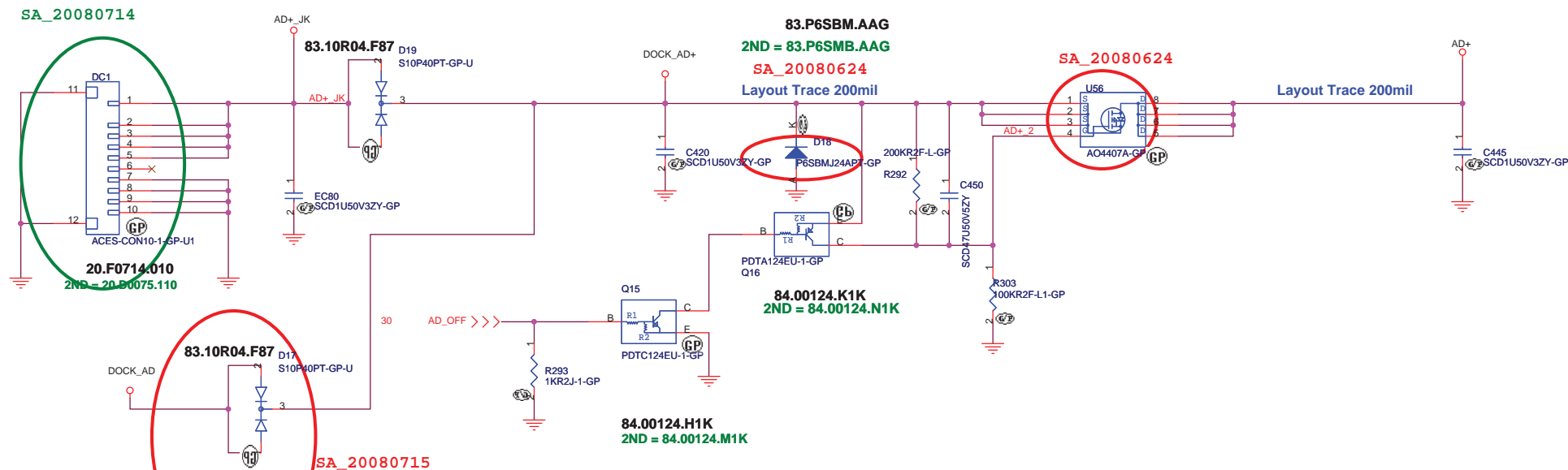


Aux Power 3D3V_AUX_S5

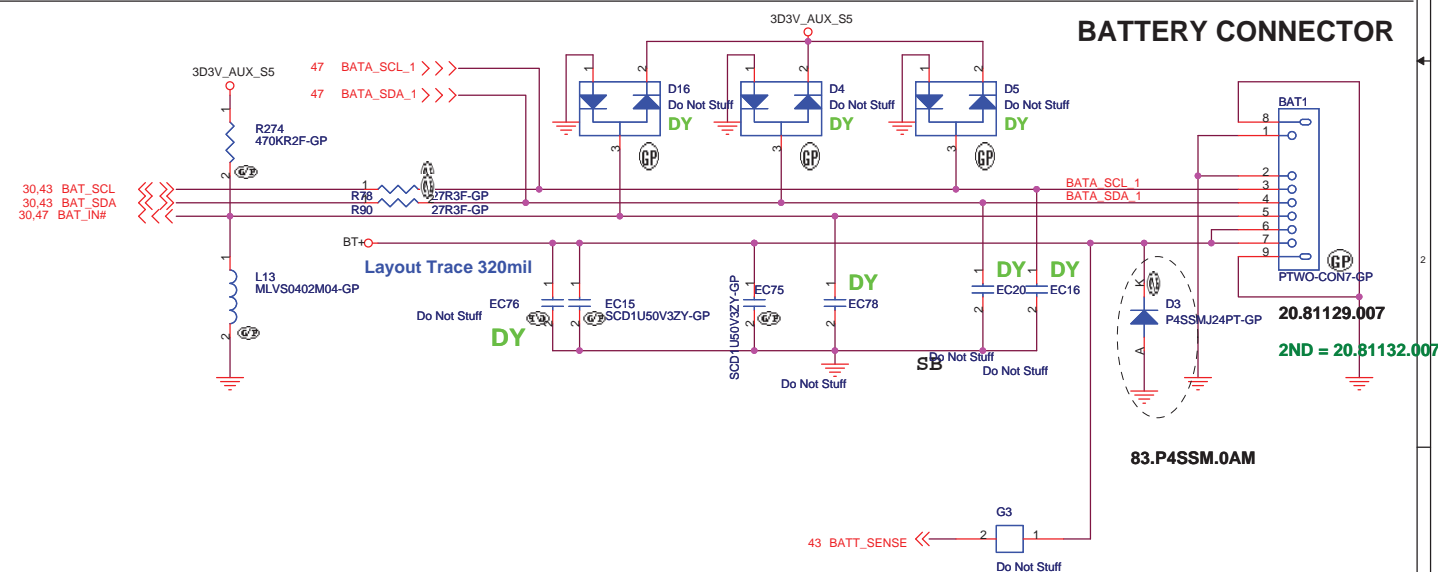




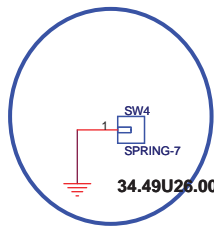
Adaptor in to generate DCBATOUT



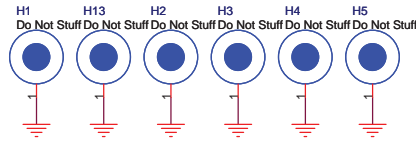
BATTERY CONNECTOR



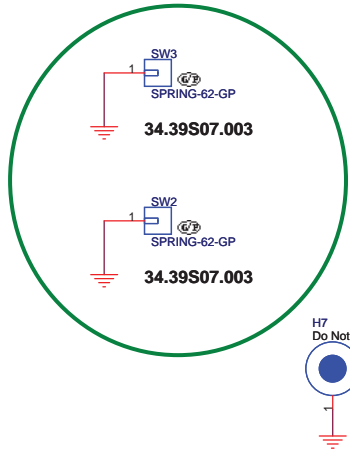
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SA_20080725



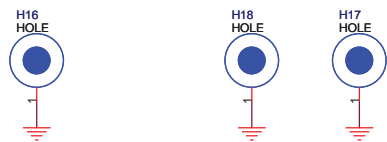
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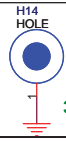
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34.41Q08.011

34.41Q08.011

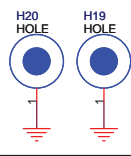


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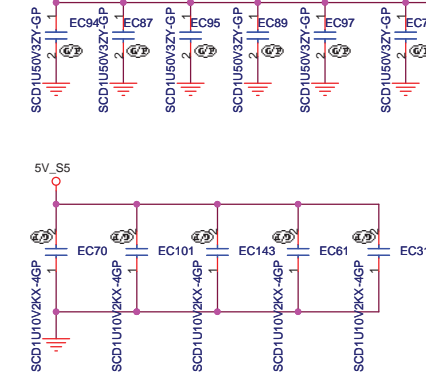
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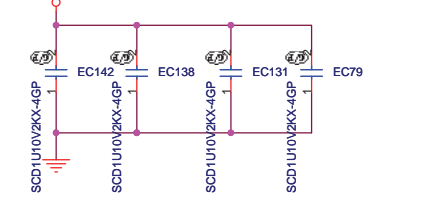


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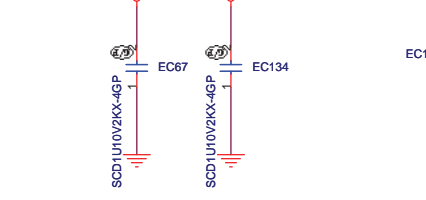
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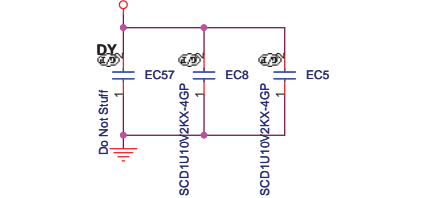
5V_S5



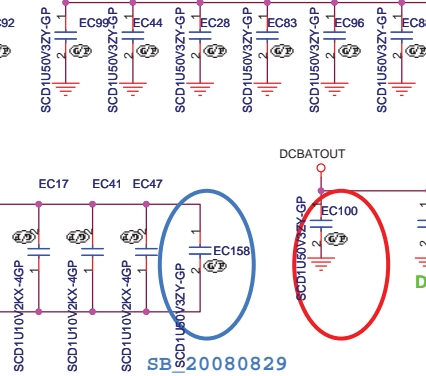
3D3V_S5



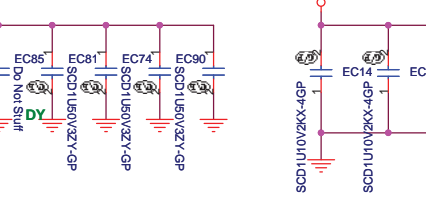
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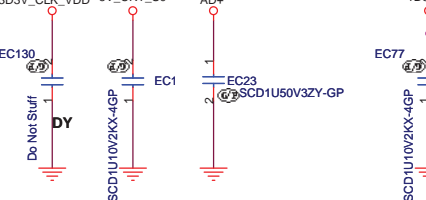
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5V_S0



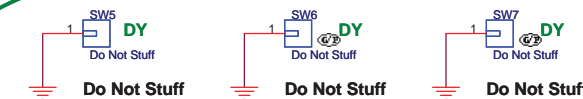
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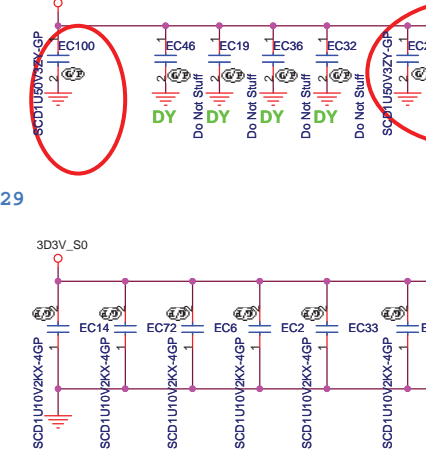
3D3V_LAN_S5



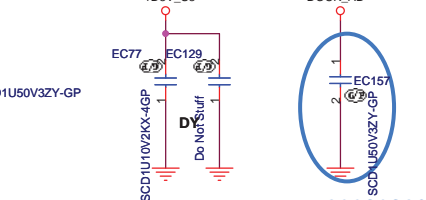
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DCBATOUT



3D3V_S0



DOCK_AD



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C

B

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Change List

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A

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-1

Date: Wednesday, October 01, 2008

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